A SIGNAL CONDITIONING SYSTEM FOR THE FOETAL ELECTROCARDIOGRAM

A Thesis Submitted
In Partial Fulfilment of the Requirements
for the Degree of
MASTER OF TECHNOLOGY

By
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to the

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY KANPUR

JULY 1975

CERTIFICATE

This is to certify that the work on "A Signal Conditioning System for the Foetal Electrocardiogram" has been carried out under my supervision and this has not been submitted elsewhere for a degree.

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ACKNOWLEDGEMENTS

I would like to express my deep appreciation and gratitude to my thesis supervisor, Dr. R.N. Biswas, for initiating me to the work presented in this report. He has found time in his busy schedule for many interesting and fruitful discussions. But for his sustained guidance and kind help in inumerable ways, the work presented would not have been possible.

I am also grateful to the Electrical Engineering Faculty in general, and Drs. T.R. Viswanathan, S.K.Mullick and V.P. Sinha in particular, for their help.

Mr. S.N.Sikdar merits my special gratitude for his help in fabrication of the unit.

My acknowledgements are also due to Mr. K.N.Tewari for his excellent typing of the report.

S.A. Halgeri

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ABSTRACT

A signal conditioning system has been designed to extract the Foetal Electrocardiogram from the skin-electrode signal available from the expectant mother's abdomen. The problems arising out of the aperiodicity of the signal, the presence of interfering maternal complexes and the accompanying noise has been solved by using (i) matched filter detection (ii) maternal complex blanking by period sampling and (iii) digital signal enhancement.

An analog signal pre-conditioning system incorporating (ii) and (iii) mentioned above has been successfully fabricated and tested with a simulated input signal. The complete design of the digital enhancement system has also been given.

Chapter - 1

INTRODUCTION

Scientists and medical researchers have tried to develop techniques and devices with which medical diagnoses can be made even before an individual's birth. Since the heart is the most important organ of a human body, it is logical that attention should be focused on the foetal heart. The best technique of studying the foetal heart condition is to observe its electrocardiogram.

The Foetal Electro Cardio Gram (FECG) is an electrical signal, associated with the beating of the embryonic heart, which can be obtained normally by applying a pair of electrodes to the abdomen of a pregnant woman during the last 6 months of pregnancy. The characteristics (presence of the signal, rate, waveshape, dynamic behaviour) of this foetal heart signal are immensely useful to an obstretician. This can help him to take the major decision about the caeserian operation or give valuable information about the foetal life in cases of early threatened abortion. In a labour room cases of prolonged labour, foetal distress, placental complications or breech presentation can be cleared faster. A medical researcher might also find it useful for studying the effects of various drugs, medications or psychological stimuli on the foetus.

Unfortunately the ECG's recorded from the abdominal wall contain a weak foetal signal, a relatively strong maternal heart signal and considerable noise. Occasionally, the foetal signal to noise ratio is so poor that even the presence of the foetal signal cannot be established from careful visual analysis of a recorded signal. The situation is particularly bad during labour when muscular activity adds more noise or during early pregnancy when the foetal heart signal is much weaker. Many schemes for enhancing the quality of foetal signals available to the diagnostician have been tried. Only recently, however, through the use of coherent averaging techniques, has an improvement in the quality of foetal signal sufficient for observation of its true nature (without the obscuring noise) been achieved.

The main aim of the work presented in this thesis is to achieve a significant improvement in the method of detection of the foetal complexes. Once the complexes are accurately detected, the presently available weighted averaging schemes can give us a near perfect enhancement. This should lead to a more precise prenatal diagnosis of the foetal heart condition.

The second chapter deals with the basics of ECG, a detailed study of the signal that we get, the desired output

and various methods to achieve the same. The design of Analog Detection System is given in Chapter 3 and the Digital Signal Enhancement System is considered in the fourth chapter. Chapters 5 and 6 deal with the actual circuit descriptions of these two units, respectively. Finally, we briefly discuss the signal simulation and storage (for testing) in Chapter 7.

Chapter - 2

PROBLEM SPECIFICATION AND ANALYSIS

Before considering the details of the FECG and the enhancement methods, let us note a few relevant points about an ECG in general.

2.1 THE ELECTROCARDIOGRAM

Electrical potentials exist across the enveloping membranes of living cells and many cells have the ability to propagate a change in these potentials. Nerve, muscle and gland cells exhibit phenomenon. When such a cell responds to a stimulus, the membrane potential exhibits a series of reversible changes which are called the Action Potentials. The muscle cells forming the heart's pumping chambers go through their contraction and relaxation cycle, which results in the circulation of blood. These cells respond to a continuous stimulus generated by the pacemaker node - the sinuatrial node. This stimulus not only goes through well defined neural paths to the heart cells but also propagates away from the heart, through the body tissues and may be detected by using a pair of electrodes attached to the skin anywhere on the body. Electrocardiogram is the plot of differential voltage between two such electrodes.

For diagnosis of heart condition by comparison of ECG's the electrode positions have been standardized. The

right ankle is always connected to the system ground and the differential voltage between the two of the particular nine positions (six on the chest, and one each on the right arm, the left arm and the left ankle) is taken. The waveform of a normal resting ECG differs from position to position. The waveform for one full period in V1 position is shown in Figure 2.1. This waveform is particularly shown because the maternal and foetal ECG's in the abdominal signal have a similar shape. This waveform is commonly referred to as a complex. A complex is divided into five portions and labelled as P, Q, R, S and T. In a complex, PQ refers to the atrial activity, RS to the compression of the ventricles and ST to the relaxation. The iso-electric interval between T of one complex and the P of the next complex varies with the beat rate. Dignosis of the heart using ECG involves observation of the shape of various portions of a complex, relative timings between them and the inclination of the cardiac vector (with a particular reference direction) which is calculated from the ECG's at all the nine standard positions (V1 to V6, AVL, AVR, AVF).

2.2 FECG SIGNAL DETAILS

An FECG is the ECG with the electrodes placed on the abdomen of a pregnant woman after about 12th to 16th week (yet undecided) of gestation. Again the ground electrode is placed on the right ankle. Positions of the

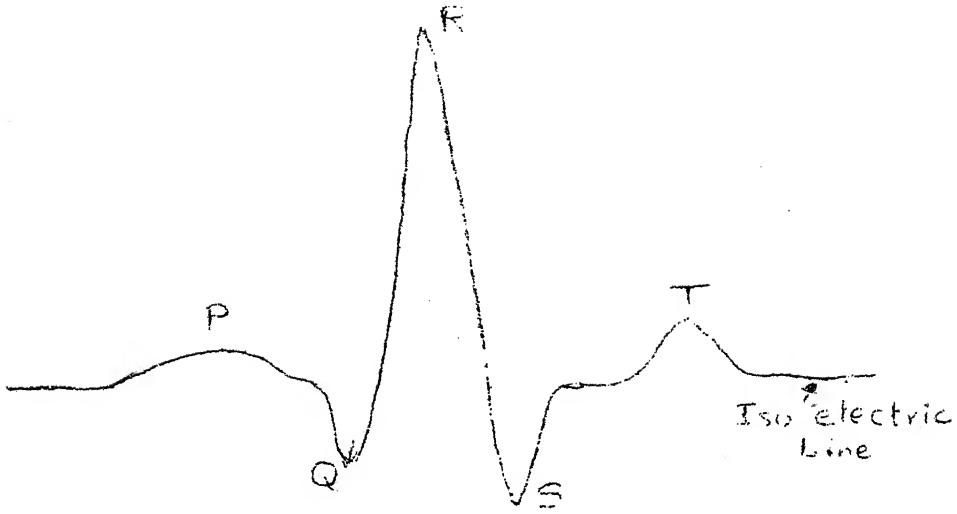


Figure 2.1: THE ECG COMPLEX

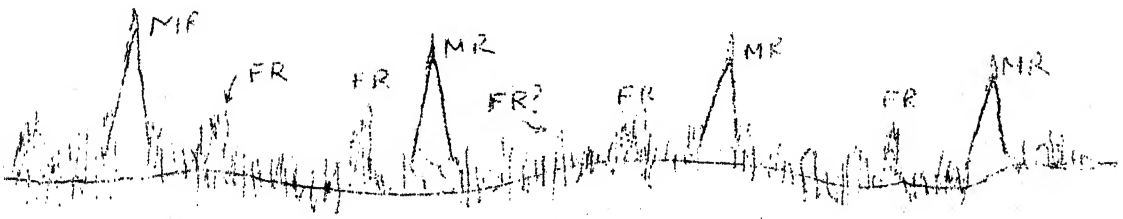


Figure 2.2: A TYPICAL ABDOMINAL SIGNAL

two signal electrodes have also been standardized [1]. Let us consider the most common midline electrode position.

The signal thus obtained will be given by

$$a(t) = r(t)\,[m(t) + f(t) + n(t)\,]$$

where,

- $a(t)$: Abdominal signal
- $m(t)$: Component from the maternal heart
- $f(t)$: Foetal heart contribution
- $n(t)$: Additive noise component - mainly muscle noise termed as electromyogram + EM interference + system noise
- $r(t)$: Multiplicative noise component - mainly due to breathing (consists of low frequencies upto 5 Hz).

Depending upon the orientation of the foetus inside the uterus, the polarity of foetal R peak (complex) may be same or opposite as that of the maternal R peak (complex). A sketch of a typical abdominal signal (with similar polarities) is shown in Figure 2.2.

We study the signal in three domains as follows:

a) Amplitude Domain : For detection, we are interested in peak levels. Thus any good quality electrode will give 100 μV or above of maternal signal and 20 μV or above of noise.

The foetal signal level will depend very much on the period of gestation [1]. In early pregnancy it is around 10μV, it increases to 60 - 70 μV during 17th to 22nd week; it drops down during the 30th week and during term it reaches to approximately 100 μV.

b) Frequency Domain : The beating rate of a human heart fluctuates on both long and short term basis. It has a pseudo-periodic nature, the degree of the fluctuations differing from one subject to another. The beating rate can at the most vary from 40 beats per minute (b.p.m.) to 300 b.p.m. [3]. Lowest rate indicates a complete heart block. However, in most of the cases the maternal rate will be between 60 bpm to 120 bpm and the foetal rate will vary between 100 bpm to 250 bpm (maximum is reached during labour).

Since we wish to extract a signal from noise, its frequency spectra is of prime importance. A typical foetal signal [2] had a 2.4 Hz fundamental, harmonic structure upto 33 Hz and notable amplitude upto 45 Hz. Power density of R wave is maximum between 15 Hz to 40 Hz for the foetus and 10 Hz to 30 Hz for an adult. Any ECG signal will totally lie between 0.1 Hz to 200 Hz.

c) The Time Domain : In a complex of an adult ECG at normal beat rate of 70 to 80 bpm, the PQ duration is 100 to 120 ms, QRS stretches to about 160 to 200 ms and the ST duration is

approximately 300 ms. The various time durations for a foetal complex are not as well established. The P & T waves of a foetal complex are attenuated due to a filtering effect of the tissue separating the foetus from the skin of the maternal abdomen. The QRS duration is usually around 60 ms and the total complex occupies approximately 160 ms. As reported by Larks and Karim [1] the base width of the R wave varies from 26 ms to 40 ms with the period of gestation (20 weeks to term).

2.3 THE BASIC REQUIREMENT AND POSSIBLE SCHEMES

A cardiologist would like to have an ON-LINE instrument giving a clean foetal ECG on a strip chart recorder, just like an adult ECG. The unit should require minimum of patient instrumentation.

Keeping this in mind we now examine the possible solutions. We have to deal with a signal which is pseudo-periodic and is totally submerged in noise most of the times. To make the matters worse, the signal is mixed up with another much stronger pseudo-periodic signal. And finally, the frequency spectra of the noise and the signal are considerably overlapping. The only usable property the signal has is that the complexes will have roughly the same shape, provided the patient remains steady. We want to get rid of the overriding noise on the complexes without distorting their shape. This

is an utmost necessity since all the information that is sought after is contained in the waveshape of the complexes. The only way to accomplish this is the coherent time averaging of the complexes. Coherent time averaging of a repetitive real-time signal consists in storing samples of the signal in a memory and then adding (with particular weightages) the value of the corresponding samples, which are equidistant in time from a particular reference. This reference point must be in the most prominent part of the signal. As more and more complexes are included in the average, noise, being random in nature, will slowly get cancelled out and the averaged complex will appear more and more clean. The extent to which the signal to noise ratio gets enhanced by this process will mainly depend upon the coherence of averaging, i.e. the accuracy in time with which the reference point on each complex is detected. Thus for perfect coherence we need perfect detection of each and every complex. Thus, the problem consists of two distinct parts, one of Reference Point Detection and the other of Enhancement.

Enhancement of the complex can be done either by digital technique or by analog technique. As the signal of our interest has got a very low repetition rate, the enhancement will involve hundreds of milliseconds of delays. Clearly, if we go the analog way, it will be hard to implement such large delays as

well as the delays will cause a serious frequency distortion of the signal. Therefore, we resort to the digital method, where delaying of a signal is not much of a problem and frequency distortion is minimum.

Let us now look into the problem of Reference Point Detection. In any ECG complex, the part that clearly stands out is its R wave. The peak point of the R wave is thus the evident choice for the reference point. In detecting the complexes we must pick up only those complexes that are not engulfed by a maternal complex. The maternal ECG is a strong signal and it cannot be disregarded as noise. As the foetal beat rate is usually double the maternal beat rate, we expect to get quite a number of such foetal complexes for a faster enhancement.

For this detection we can make use of the properties of the signal in amplitude, frequency or time domain. We now consider them one by one.

If we utilize the amplitude domain properties of the signal, the scheme turns out to be pretty simple. The vastly different peak levels of the R waves of maternal and foetal complexes are sensed by two threshold comparators and the undisturbed foetal complexes are picked out by means of appropriate logic. The maternal R waves always go above the

peak noise level and can thus be reliably detected with a threshold comparator. But the necessity of the foetal R waves also going above the peak level of the noise imposes a serious restriction on the period (of gestation) in which this scheme can be used. In order to separate the foetal R peaks from noise peaks it is required that the foetal signal to noise ratio be above 1.5. Thus we drop the threshold detection scheme.

We can make use of the approximate periodicity of ECG signals to the detect the complexes with the help of a phase locked loop. Since we have two periodic signals mixed up we have to use two separate PLL's to lock with them. If the composite signal is fed to the foetal PLL directly, we can never expect it to lock to the foetal signal since the maternal signal is so strong and the maternal and the foetal signal frequency spectra are totally overlapping. In the case of the maternal PLL , we can easily separate the peak portions of the maternal R waves and use them to lock with the PLL. The VCO signal can then be made use of to produce maternal windows wide enough to blank each and every maternal complex. The signal can now be applied to the foetal PLL. But the most unfortunate part of this blanking process is that it invariably suppresses at least one foetal complex in three. This results in making the foetal signal strongly aperiodic irrespective of whether it is originally periodic or not. It would be very

difficult or even impossible to make a PLL lock to such a signal. There are some minor (relatively) difficulties also, like both the PLL's should be in a locked condition simultaneously. This is especially hard to achieve during labour when both the maternal and foetal beat rates fluctuate tremendously and that too in very short intervals of time. If these fluctuations lead to multiple harmonic locking of the maternal PLL then some of the maternal complexes will be let into the foetal PLL and the system will never work. Lastly, the variations in the phase error of the foetal PLL will drastically affect the coherence of averaging and hence the quality and speed of enhancement. Alternatively, one can think of the fixed-delay time domain autocorrelation technique for the detection. But here again, similar time domain properties of the two complexes force us to blank the maternal signal, the resultant aperiodicity of the foetal signal making the fixed-delay autocorrelation impossible to use. Therefore since maternal blanking is unavoidable use of any scheme which banks on the periodic nature of the signal is not advisable. We want to extract a signal from noise, assuming that the signal is aperiodic. Thus we are left with the only time domain property of the signal, which distinguishes it from noise, that is the waveshape of the complexes. Thus, we logically turn to a special type of autocorrelation - that is the Matched Filtering. We discuss this in greater detail in the next section.

2.4 THE MATCHED FILTER

A matched filter is a special kind of filter which is matched to a particular waveform, so that, when such a waveform appears at its input with noise it gives a significant improvement in the signal to noise ratio. In other words, it gives an indication at the output in the form of a detect pulse having a large peak amplitude in comparison to noise, whenever the waveform to which it is matched, appears at the input. The matching condition requires that the impulse response of the matched filter should be the time inverse of the waveform to which it is matched. Now the realizability conditions of a filter force us to put a delay in this matching. This delay appears as the delay between the waveform appearing at the input of the filter and the detect pulse appearing at the output. This detection delay is the property of the filter, since it is related to its impulse response and is independent of the frequency domain properties of the signal. Thus the matched filter responds to the waveform irrespective of its repetition rate, provided that the output pulse generated by one waveform settles to almost zero value before the next waveform appears. (When related to our terms, the matched filter will not operate beyond a beat rate of 600 bpm. This is almost double the maximum possible beating rate of a human heart.)

This matched filter technique is sort of a 'fixed waveform' autocorrelation, where the waveform with which the

signal is correlated is "stored" inside the matched filter. No sooner that particular waveform appears at the input the matched filter presents us with an indication which is sure to be picked up.

Thus after the maternal blanking we apply the signal to the matched filter and its output is threshold detected and then peak detected to get the marker for enhancement. The detection delay can be easily compensated by a shift register of appropriate length once the signal is digitized. A matched filter can thus solve our detection problem.

2.5 THE MATERNAL BLANKING SCHEME

As far as the generation of maternal blanking windows is concerned, we do not have the noise rejection problem. Hence the Maternal Synchronizing Pulses (MSP) generated by sensing the maternal R peaks can be used in conjunction with a period sampling method to generate the maternal blanking windows(MBW). Using this method we can reliably blank each and every maternal complex, although at times when the maternal period fluctuates, the width of the blanking window might become a bit more than necessary.

We can now proceed with the system design in the next chapter.

Chapter - 3

DESIGN OF THE ANALOG DETECTION SCHEME

After deciding on the detection scheme in the previous chapter, we can now decide on the various blocks that are needed for processing the signal. The block diagram is shown in Figure 3.1. First we will briefly consider the required blocks and then discuss about the specifications of each block.

The input is a differential signal having a few micro-volts of peak amplitude at an impedance level of several hundred kilo-ohms. So the front end of the unit will be a high-gain high-input-impedance DIFFERENCE AMPLIFIER having a differential input and a single ended output. This output is fed to the MATERNAL COMPARATOR to get the maternal synchronizing pulses. These pulses and the signal are given to the Maternal Blanking circuit. The output of this MATERNAL BLANKING CIRCUIT is amplified if required and then applied to the MATCHED FILTER. Depending upon the polarity of the foetal R peak, either the output of the matched filter as such or its inverted version is fed to the CLIPPER AND PEAK DETECTOR. To indicate, just the presence of the foetal signal (but not the beat rate) we now feed the detect pulses (output of the peak detector) to drive a LIGHT EMITTING DIODE for visual indication, and a SPEAKER for audio indication. This is

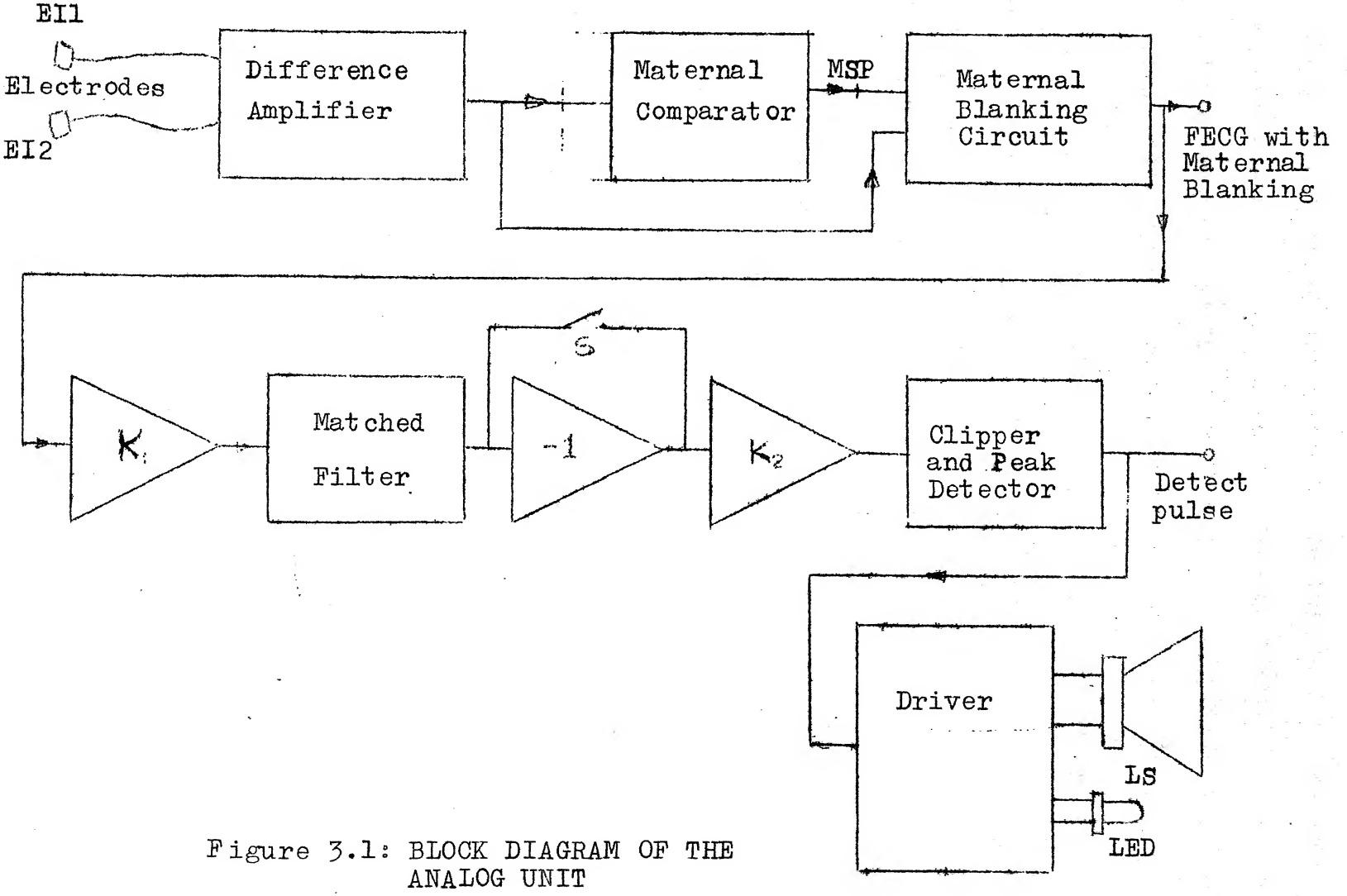


Figure 3.1: BLOCK DIAGRAM OF THE ANALOG UNIT

sometimes valuable in the sense that it gives audible evidence to the expectant mothers that her pregnancy is continuing satisfactorily, especially in case of patients who have suffered in their previous pregnancy.

The detect pulse and the FECG signal after maternal blanking will thus form the outputs of our analog unit. These signals will be required for the digital signal enhancement. We will now discuss the requirements of each block.

3.1 THE DIFFERENCE AMPLIFIER

We will consider its specifications step by step.

(a) The differential gain: With reference to data in Sec.2.2(a) we usually get a maternal R peak level of 0.1 mv with good silver electrodes and an electrolyte paste to reduce the skin resistance. Since the maternal R peak has the highest amplitude in our signal it should reach the peak at the output for optimum use of the dynamic range of the amplifier. If we use $\pm$ 12 volts as the power supplies, we should have a gain of 100 dB to get a R peak of 10 volts at the output. As the input signal level will differ from one subject to another we will keep the gain variable around 10^5.

(b) The input impedance: The ECG signal is formed by the potential variations on the skin which are picked up by metal electrodes in contact with the skin. This contact has to be as perfect as possible so that the impedance level of the signal is low. The metal should be a good conductor of electricity

with sufficient area. Usually silver electrodes are used so that the loss of contact due to rusting is avoided. No hair should come in between the electrode and the skin. An electrolyte paste is rubbed on to the skin and then the electrode is tied on it with a rubber strap. The electrolyte goes into the pores of the skin which increases its conductivity and also makes a homogeneous contact with the electrode. The electrolyte should be of a type that is suited to the electrode material.

With all these precautions one is able to reduce the electrode resistance to a few hundreds of kilo-ohms. The input impedance of the amplifier should therefore be of the order of 10 megohms or more. In addition to this, the amplifier has also got to have a low output impedance and a high CMRR.

(c) The pass band : We try to reduce the noise as much as possible by keeping a minimum passband. The low frequency breathing noise goes upto 5 Hz while fundamental frequencies of maternal and foetal signals are greater than 1 Hz (Ref. Sec. 2.2b). On the high frequency side, the spectrum of the FECG sgsignal extends up to 200 Hz. A reasonable choice of the pass band is thus 1 - 200 Hz. The upper cutoff is marginally chosen to curb the tendency of oscillation of the high gain amplifier.

3.2 MATERNAL COMPARATOR

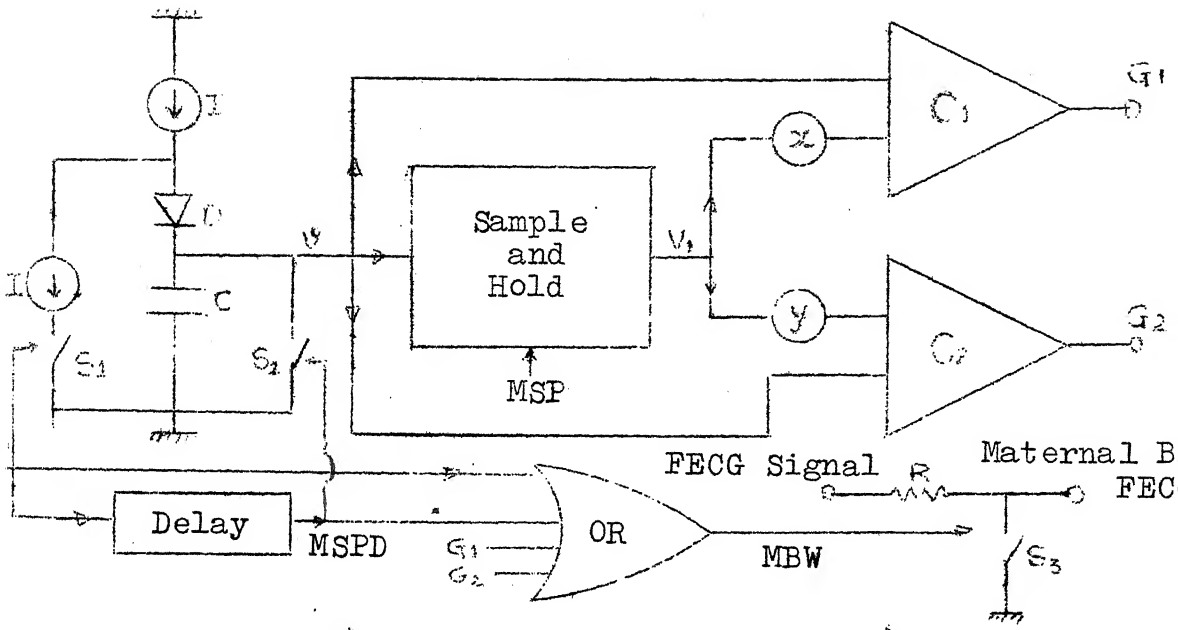
In our signal the maternal R peaks would go beyond 10 volts (unless clipped due to saturation) while the foetal R peaks and the noise would be in the range of 3 to 4 volts at the most. (Electrode positions can be adjusted to get this situation if required.) The clipping level should be such that the MSP's be wide enough so that minimum expansion is required to generate the MBW's. At the same time the level should not be so low that any thing, other than maternal R peaks will be sensed. Thus we keep the comparison level around 6 volts adjustable with a trimmer. The comparator should have enough hysterisis so that the overriding noise, if any, on the maternal R peaks may not produce multiple synchonizing pulses.

3.3 THE MATERNAL BLANKING CIRCUIT

The function of this scheme is to expand every MSP on both the sides so that the significant part of the maternal complex, mainly QRS, can be blanked. Usually, P & T sections are merged into the base line noise. We cannot afford to blank P & T as this will drastically reduce the duty cycle of a useful FECG signal, PQ & ST durations being comparatively large. Assuming that R peak is triangular, at a 6 volt comparator level we will get MSP's around 60 to 80 ms wide. The QRS duration (Ref. Sec.2.2c) is 160 to 200 ms wide. So the MBW's should be at least 200 ms wide symmetric around MSP's.

Occasionally we might be required to blank the T wave also. Thus an independent adjustment of the leading edge and the trailing edge of MBW's is desired. This circuit must have some form of memory as it needs to anticipate the position of the MSP's in order to form the leading edge of the MBW's.

Figure 3.2 shows the scheme in full detail. We store the information of one period and use it to anticipate the position of the next pulse. For this we need to convert time to voltage with a linear sweep. The voltage'v'can be sampled with the help of MSP and held till the next MSP comes. V_1 is one such sample. With the help of two comparators (C_1 & C_2), two attenuators (x & y) and an OR gate we can generate the MBW. x will control the leading edge and y, the trailing edge. We include the MSP in the inputs of the OR gate as a precaution. The discharge pulse MSPD should be just enough wide so that the capacitor C is discharged from the maximum value of'v' to zero volts. Else it may affect the linearity of time to voltage conversion. The values of x and y remaining fixed, the width of MBW will increase linearly with the increase in the period, the duty cycle of the blanked FECG signal remaining constant. Thus we set the MBW width to the minimum required value and when the maternal period attains its maximum value (120 bpm, 0.5 sec.). This will guarantee the blanking of each and every maternal complex.



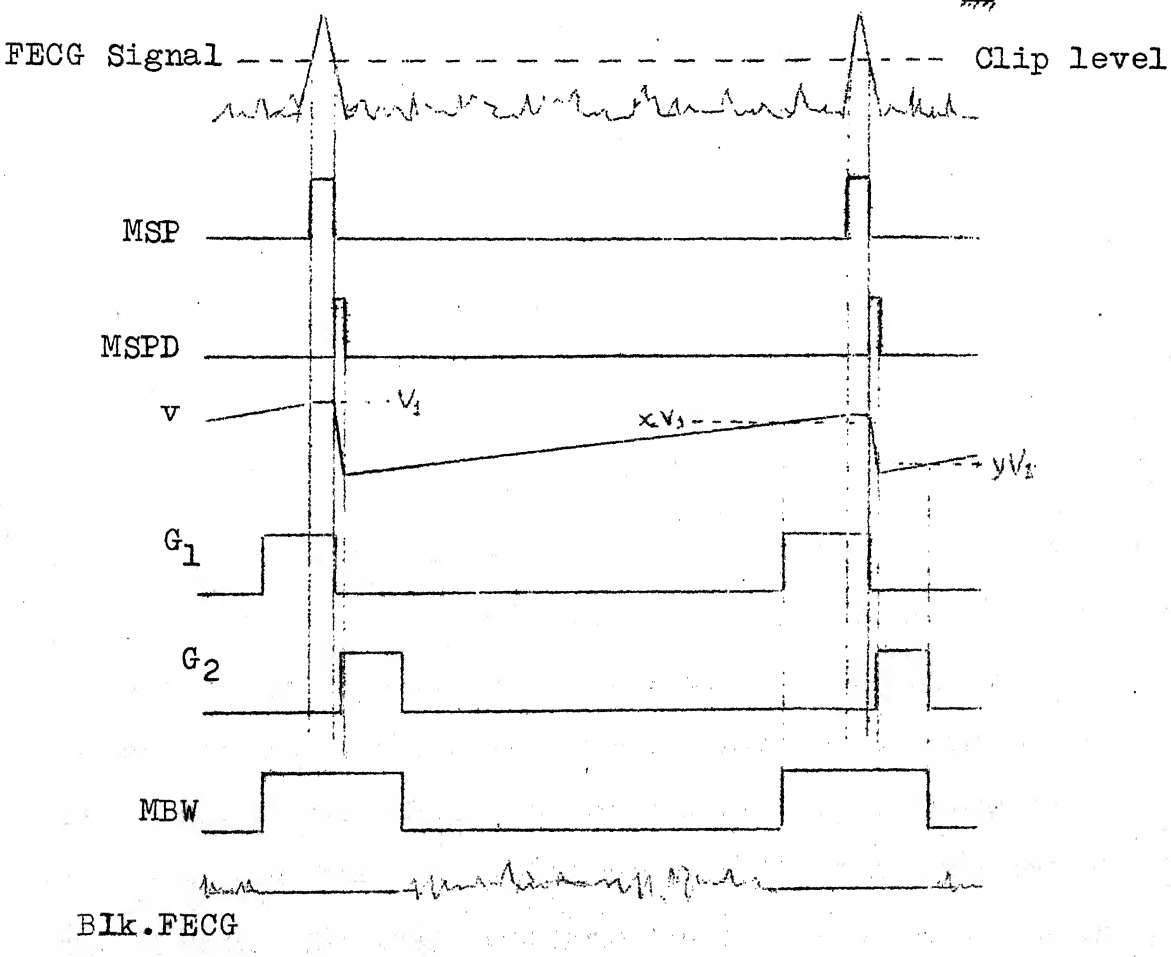


Figure 3.2: THE MATERNAL BLANKING SCHEME.

3.4 THE MATCHED FILTER

The theory of matched filters is quite well known. However, the relevant portions of the same are summarised in Appendix A1.

Much of the tedium of filter design has been eliminated by the excellent work of several contributors who have tabulated element values, pole locations, polynomial coefficients and other pertinent design data for several conventional types of filters. Henderson and Kautz have published [7] transient responses for some of the standard types of filters, plotted on the IBM 650 computer. Since we are searching for a filter having a spedific impulse response it would be worthwhile to have a look into these plots.

If we start searching for a filter having an impulse response resembling TSRQP (time inverse of PQRST), we will need summing of two impulse responses (TS & RQP) with a delay of hundreds of milliseconds. This is undoubtably a tough job. Such an exact matching is not really desired, since the time durations and waveshape of the complex are going to vary a little bit from one foetus to another. In other words, the matched filter should have enough tolerance to enhance a narrow band of waveshapes symmetric around its impulse response. Thus we assume that a complex essentially consists of only PQR part (R being the most important) and search for a filter

having an impulse response resembling RQP. Clearly, this is a low pass impulse response. In general the R peak is a symmetric pulse , thus looking at the shapes of the first peak in the impulse responses of Butterworth, Chebyshev and Bessel filters of first ten orders, we choose a 4th order low pass filter. The first-peak waveshapes of first three orders are totally asymmetric.

We want only one cycle of ripple (Q & P) after the first peak. Butterworth gives two , Chebyshev gives three or more and Bessel gives none. Butterworth filter seems to be closest to our requirement. Considering the simplicity in hardware we select a 4th order Butterworth filter as our matched filter. Figure 3.3 shows the plot of the impulse response and Figure 3.4 , the pole locations of our matched filter.

3.4.1 The Break Frequency:

We must now find the break frequency ω_o of the filter. The impulse response plots are normalized with respect to both amplitude and time. We do not bother about the amplitude scaling or impedance scaling since we are going to use active filters.

Let $g_n(t)$ and $g_o(t)$ be the impulse responses of the normalized filter and the practical filter, respectively;

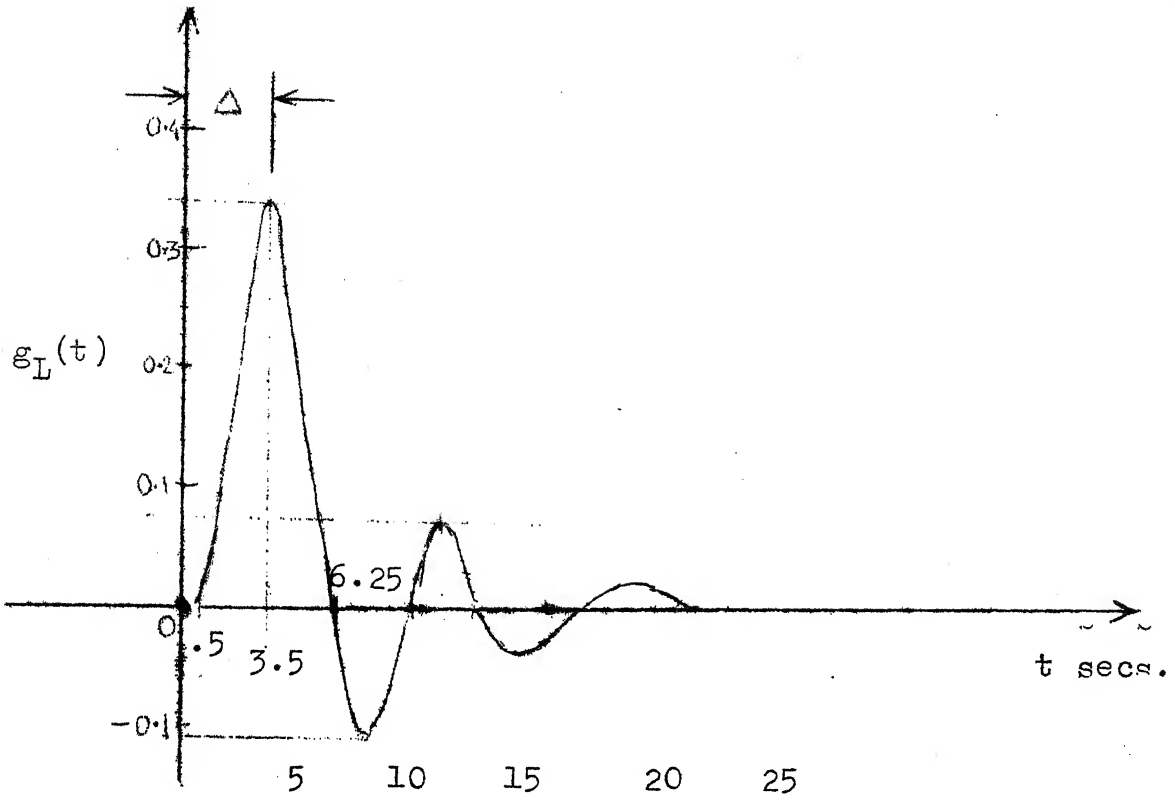


Figure 3.3: PLOT OF THE IMPULSE RESPONSE OF THE 4TH ORDER LOW PASS BUTTERWORTH FILTER

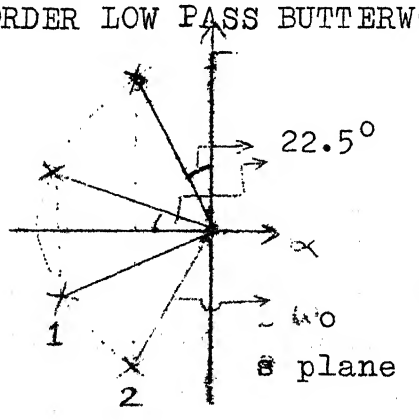


Figure 3.4: POLE LOCATIONS OF THE MATCHED FILTER.

$G_n(s)$ and $G_o(s)$ be their transfer functions, respectively and ω_o the break frequency of the practical filter. The normalized filter has a unit angular cutoff frequency and unit impedance level. Thus,

$$G_o(s) = Z_o\, G_n(\omega_o\, s)$$

and $$g_o(t) = (Z_o/\omega_o)\, g_n(t/\omega_o)$$

We will have to rescale the time axis by a factor $1/\omega_o$. Since R peak is the most prominant part of a complex, we use its base width as a matching criterion. Referring to Sec. 2.2c we note that the average base width of a foetal R peak, considering the variation with the period of gestation, is 34 milliseconds. The first peak base width of the normalized filter as measured on the plot (Figure 3.3) is 5.75 secs. Thus,

$$\omega_o = (5.75/34) \times 10^3 = 162.3 \text{ rps.}$$

3.4.2 The Detection Delay:

The expected detection delay A is the time duration between t=0 (y axis) and the first peak of the impulse response. As measured on the plot, it is 3.5 secs. After rescaling

$$A = 3.5 \times \frac{34}{5.75} = 20 \text{ ms.}$$

This is the expected delay between the peak point of the output pulse and the peak point of the R wave of a foetal complex.

As usual we realize this filter with two second order filters in cascade. With reference to Figure 3.4, the quality factors of the two filters are $Q_1 = 0.6$ and $Q_2 = 1.25$.

3.5 CLIPPER AND PEAK DETECTOR

Since the output signal level of the matched filter will vary with the foetal signal strength at the input, the clipping level of the clipper will have to be adjusted experimentally. Its function is to clip the base noise and permit only the highest peaks in the matched filter output to go in for peak detection. The peak detector circuit should give a pulse (an edge) at every peak it receives, with ± 1 ms. as the sampling rate of the A to D conversion will be around 2.5 ms.

In Chapter 5 we give the hardware details of the Analog Detection System.

Chapter - 4

DESIGN OF THE SIGNAL ENHANCEMENT SYSTEM

Broadly, the digital unit will consist of an A to D converter, a D to A convertor for display and the Signal Enhancement System (SES). We will first consider the main part, i.e. the SES.

4.1 WEIGHTED AVERAGING SCHEME

Basically the technique of coherent time ageraging involves the additive combination of repeated samples of the signal in such a way that the true signal reinforces itself while the noise tends to cancel out. In order to obtain coherence, the samples must be taken with the same time relationship to the signal, beginning just before the portion of the signal which is to be enhanced. The detect pulse from the analog unit will indicate the peak point of the R wave with a delay A. This will be our marker pulse for the averaging operation.

For the weighted averaging scheme a variable weighting factor is defined, represented by the symbol M. Each new average A' is composed of (M-1)/M times the old average A plus 1/M times the current sampled value S* of the true signal S.

Symbolically,

$$A' = (M-1/M)A + S^*/M \qquad (4.1)$$

Hence, if we denote the increment in the average by δA, we have

$$\delta A \triangleq A'-A = (S^*-A)/M \qquad (4.2)$$

Comparison of eqns.(4.1) and (4.2) shows that it is more convenient as well as computationally accurate to calculate A' by first determining δA from eqn.(4.2) and then adding it to A, rather than to use eqn.(4.1) directly, because two multiplications are thereby replaced by one division by a constant M.

The signal present after n complexes have been included in the average may be shown to be [8]

$$A_n = S[1 - (1 - 1/M)^n] \qquad (4.3)$$

wherein the true signal S is assumed constant through out the n complexes. The noise present along with the complexes will add only in rms sense and after n complexes, it will become [8]

$$N_n = N\{ [1-(1- 1/M)^{2n}]/(2M-1)\}^{0.5} \qquad (4.4)$$

where N is the noise level also assumed constant.

As $n \to \infty$, the signal to noise ratio that may be obtained is given by [8]

$$A_n/N_n\Big|_{n\to\infty} = (2M-1)^{0.5}\ (S/N) \qquad (4.5)$$

Eqn.(4.5) shows that with a larger value of M we get better improvement in the signal-to-noise ratio. But the assumption that the signal remains constant during the infinite averaging interval is not totally correct. Significant transient changes in the shape of the foetal complex do appear from time to time, and persist for 20 to 30 successive complexes, once they appear. For diagnostic purposes there is a need to show these transient changes in the foetal waveform, as well as to provide signal-to-noise enhancement. Thus, M should not be so large that the short term changes in the foetal complex are subdued. By adjusting the weighting factor, however, the user can obtain a variable trade off between S/N improvement and dynamic response.

We choose the value of M in powers of two as it simplifies the divider hardware. According to Rhyne [8] a maximum value of 256(2^8) is sufficient for enhancement. Hence we take M from 2 to 256.

Thus we need two memory blocks to store the old average and the new sample, plus an arithmetic unit implementing eqn.(4.2). We will use serial arithmetic, which reduces the hardware in general and is most suitable for coherent averaging. Obviously, the two memory blocks will be formed by two static shift registers (sequential access memories) the Memory Shift Register (MSR) for the average and the Sample Shift Register(SSR)

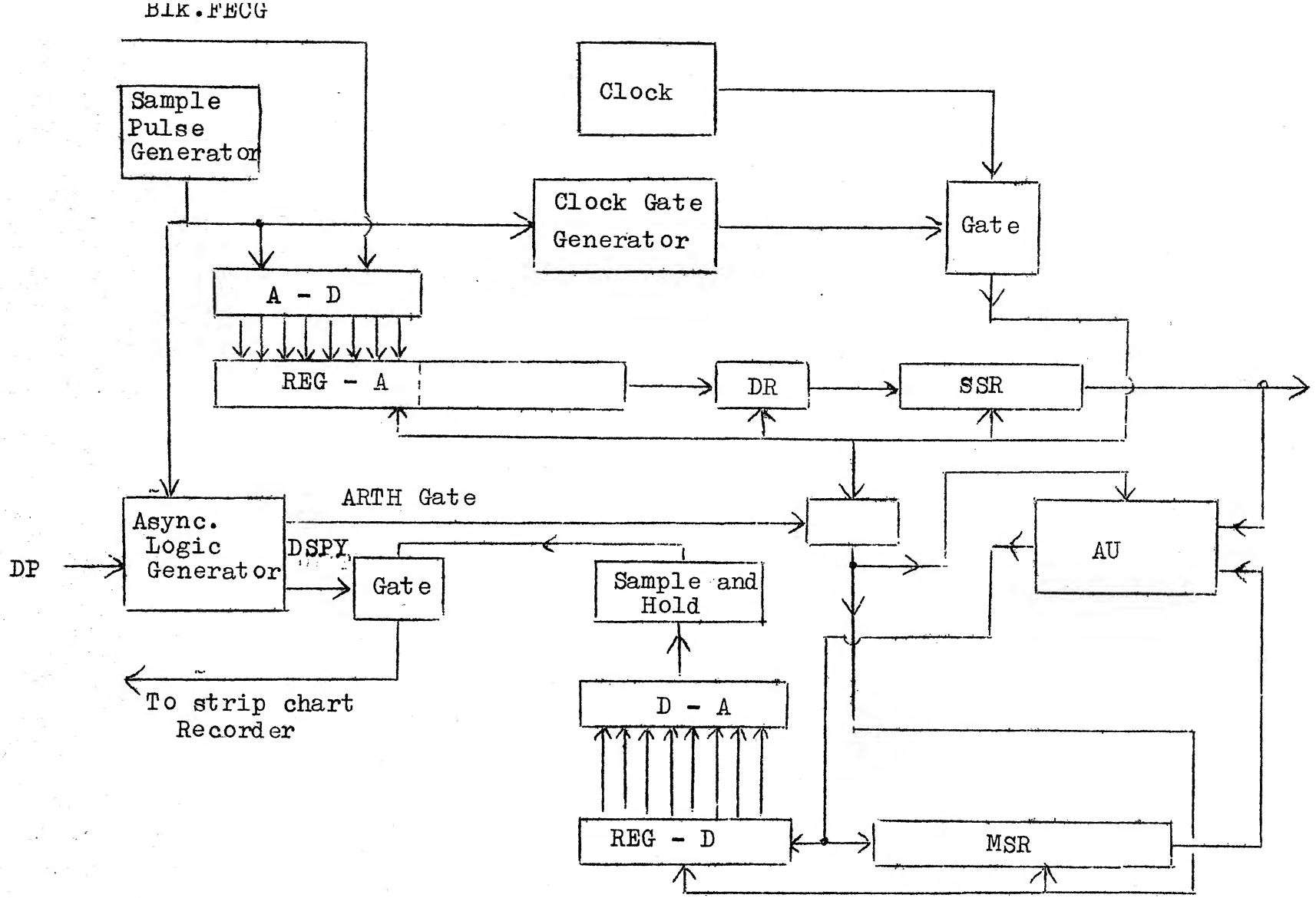


Figure 4.1: BLOCK DIAGRAM OF THE DIGITAL UNIT.

for the sample. Now we can easily compensate the detection delay of the matched filter by putting a Delay Register (DR) of appropriate length before the SSR. The A to D converter will degitize the maternal blanked FECG signal, once a sample pulse triggers it.

Normally when no new sample (complex is detected, the signal gets spilled out of the SSR. Thus every sample pulse triggers a clock gate generator which in turn gates-in a clock burst corresponding to a word shift to SSR and DR. A Detect Pulse (DP) indicates that half the complex has entered SSR. Every detect pulse starts a counter in the asynchronous logic generator, which counts the sample pulses till the full complex is let into SSR, then opens the arithmetic gate so that the clock bursts are let into AU and MSR for a full 'complex duration'. With a little delay (explained later) it also lets the D to A output to be connected to the strip chart recorder. Thus for every undisturbed (unblanked) complex at the input, we get a newly averaged complex at the output. Full block diagram of the digital unit is shown in Figure 4.1.

4.2 SPECIFICATIONS OF THE DIGITAL UNIT

We now discuss some important factors concerned with the digital unit.

4.2.1 The Sampling Rate:

The spectral analysis of FECG complexes gives the Nyquist rate as 90 samples per second. We take a sampling rate of 2 to 3 ms

which is well above the minimum requirement. Variation in the sampling rate is required for accurate adjustment of the analog detection delay in the digital unit.

4.2.2 The Word Size of MSR, SSR and DR:

We want to compensate a delay of approximately 20 ms. Thus we take a DR of 8 words so that a sampling rate of 2.5 ms will give us the required delay. The SSR and MSR should be long enough to contain 160 ms complexes. Thus we take SSR and MSR of 64 words (available value) so that the requirement is satisfied at a sampling rate of 2.5 ms. A little trimming of the sampling rate (which will be done at the start) will not seriously affect the'time content' of SSR and MSR.

4.2.3 Number of Bits per Word:

Since 8 bits/word will give sufficient accuracy for a pen recorded output and 8 bit A to D and D to A are available commonly, we choose a word size of 8 bits during conversion. But after that, to prevent the loss of accuracy due to round off errors in the arithmetic unit, we add 8 more low order bits (as maximum value of M is 256). This will make the total word size equal to 16 bits for the SES as a whole. This figure is also good from the point of view of hardware. The need of adding low order bits is explained below.

With reference to eqn.(4.2), we observe that if the word size is kept as 8 bits then A, δA and S^* will all have

8 bits/word. As explained in Chapter 6 we will implement the division by simple shifting , the number of shifts being equal to $\log_2 M$. Thus for M = 256 we will have to shift 8 times, and hence δA will always be zero. Thus no enhancement will be possible. This of course is an extreme case , but for lower values of M there will be a loss of accuracy which will introduce a dead zone into the calculation of δA. Hence we add the lower order bits to each word after A to D conversion.

4.2.4 The Clock Rate:

As explained earlier and in Chapter 6 , we need 17 clock pulses plus A to D conversion time after every sample pulse. The minimum value of sampling rate is 2 ms. A to D conversion time is say at the most 40 μs (1 clock period) then 40+17T < 2000, where T is in μs. We take a clock frequency of 25 KHz which is well above the minimum limit.

4.2.5 Arithmetic:

We need addition , subtraction and division in our AU. We use 2's complement code , which simplifies (in terms of hardware) the above mentioned operations. In a word, the lowest significant bit will be at the front while sign bit will come at the last.

The hardware details of the digital unit is dealt with in Chapter 6.

Chapter - 5

ANALOG UNIT - HARDWARE DETAILS

In this chapter we will briefly describe the various circuits which have been used to implement the system designed previously.

5.1 THE FECG DIFFERENCE AMPLIFIER

This FECG unit is supposed to extract a waveshape that is submerged in noise. Naturally, if the signal is to be amplified anywhere during the processing, the amplification should be perfectly linear. Hence we use op.amps. wherever the signal level is to be boosted up.

Figure 5.1 shows the entire pre-amplifier circuit that has been used. Since the differential amplifier made out of an op.amp. gives asymmetric input impedances, we must put two separate buffers on two lines. Also, a differential amplifier will never be able to give the magnitude of input impedance we desire to have.

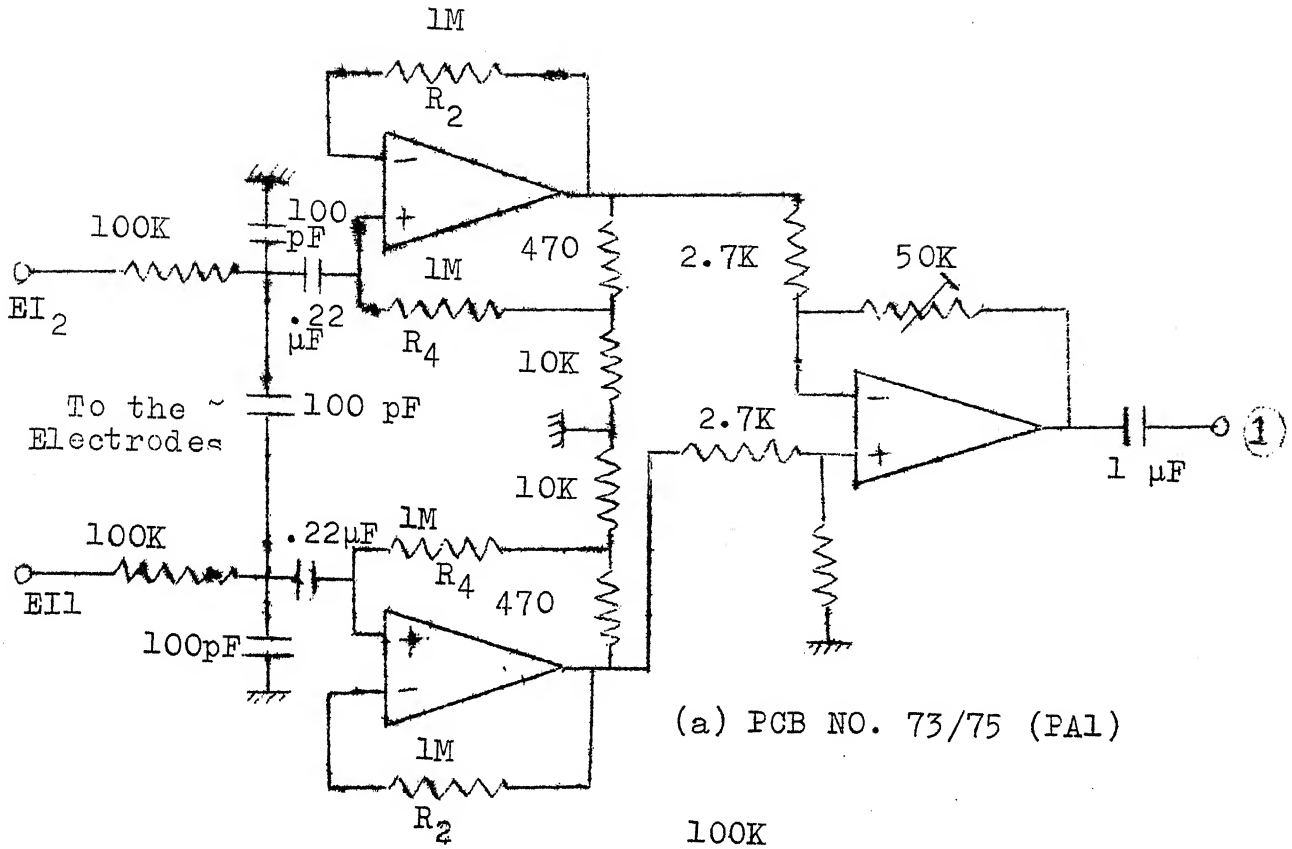
A voltage follower is a simplest buffer. But, with a follower, the bias current of the noninverting terminal will be drawn from the electrodes. This will drastically reduce the d.c. input impedance of the circuit. Thus we use a boot-strapped buffer and couple the electrodes capacitively. The

division of the output before positive feedback ensures the stability of the buffer. Thus the effective input impedance will be

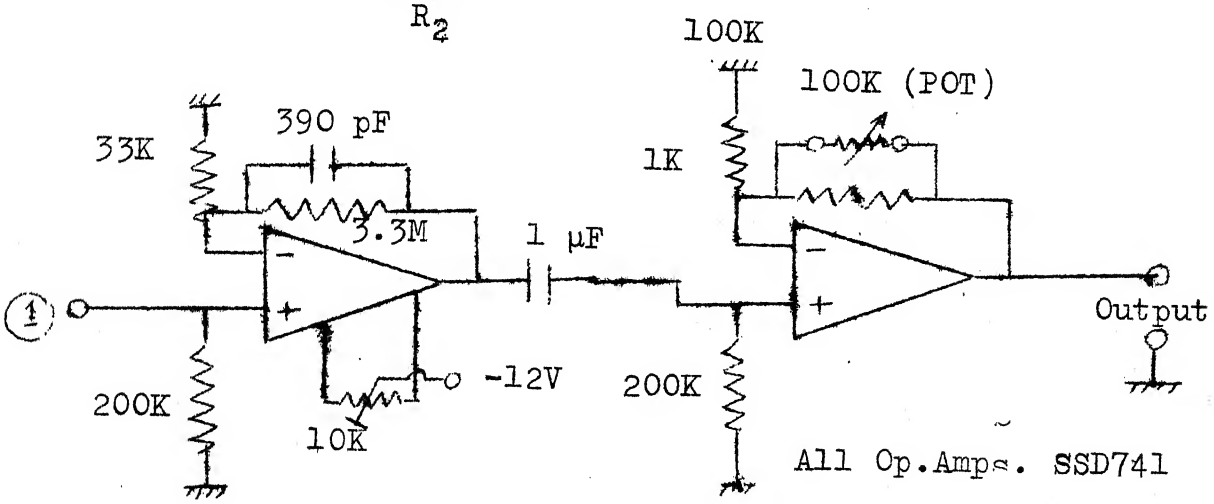
$$R_i = (1 + A)\ R_{op.amp.} \ // \ R_4/(1-A_v)$$

where A_v is the gain from noninverting input to the divider point. For the values shown, $A_v = 0.95$ and hence $R_4/(1-A_v) = 20$ MΩ We keep $R_4 = R_2$ (R_4 >> divider equivalent resister) for bias current compensation. The observed input impedance was more than 12 M Ω. Hence $C_h = 0.22$ μF will ensure that the high pass break point is less than 1 Hz. The three 100 pF capacitors at the input supress the oscillations while 100 KΩ resistors swamp the variations in the electrode resistance to some extent.

The main function of the differential amplifier is to give a good CMRR. Thus we do not extract a large gain out of it. The gain will be distributed in last three stages as 10, 100 and 100, gain of the last stage will be kept variable (panel control). The 1 μF coupling capacitors prevent the d.c. drift from getting amplified and also cut the breathing noise below 1 Hz. The low pass filtering in the 4th stage is again meant for supressing the oscillations. This circuit has been split into two PCB's one with high R_i and low gain (Figure 5.1a) and the other with low R_i (relatively) and high gain. This is to prevent the oscillations due to proximity at the edge connector.



(a) PCB NO. 73/75 (PA1)



(b) PCB NO. 20/75 (PA2)

Figure 5.1 THE DIFFERENCE AMPLIFIER

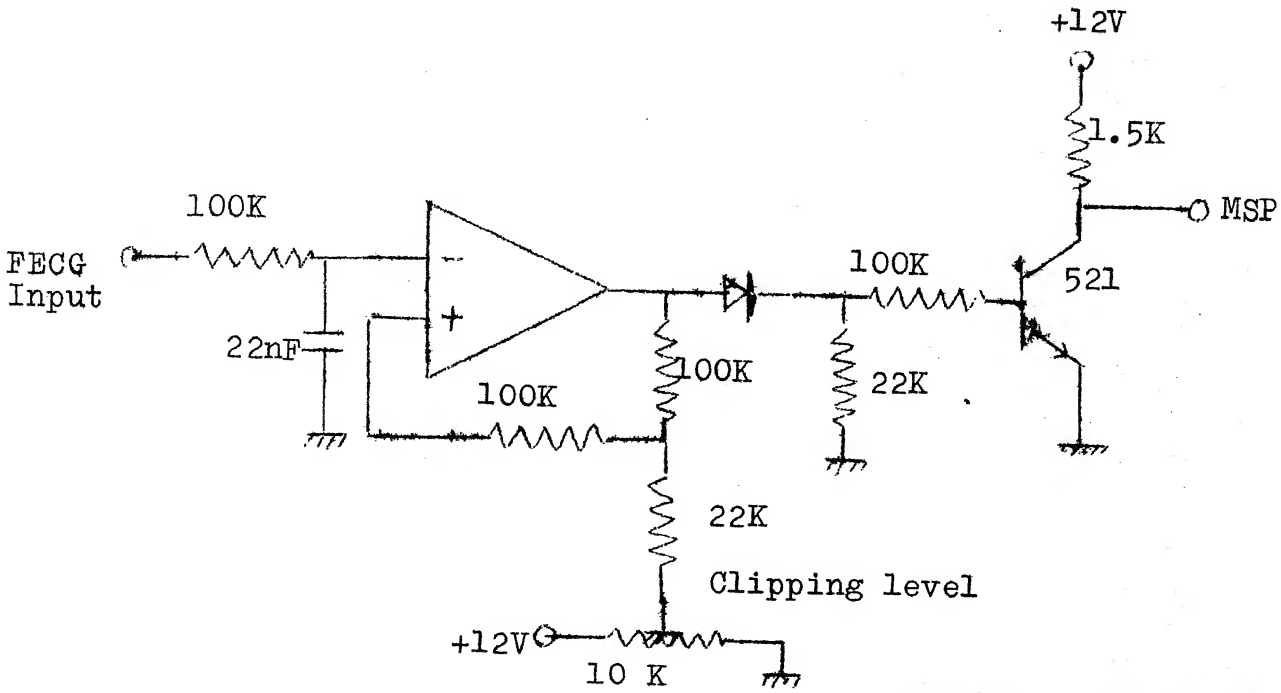


Figure 5.2: MATERNAL COMPARATOR

5.2 COMPARATOR

We use an op.amp. Schmitt trigger to get an independent control over the hysteresis and the trigger level. With the values in Figure 5.2, we get a hysteresis of around 4.8 volts. This should prevent the generation of multiple pulses due to noise overriding the maternal R peak. The 22 nF capacitor at the input filters the noise spikes to some extent. The 10 KΩ trimmer can vary the trigger level over full range of 12 volts. Normally, it will be adjusted to around +7 volts.

5.3 MATERNAL BLANKING CIRCUIT

Figure 5.3 shows the entire circuit for blanking of the maternal complexes. A transistor pulse stretcher gives a delayed MSP of around 10 ms wide, as required. The value of C is chosen as a compromise between the loading of the capacitor and its leakage resistance. It should also give a reasonable value of current (around 1 mA in our case) for the current source. The base resistance of the holding transistor (across the diode and the capacitor) is purposely kept high, so as to shunt only the required amount of current. A gate of +12 volts to -6 volts is provided for the FET switches in the sample and hold. The 1 μF capacitor in the sample and hold is large enough to hold the charge for a second and small enough for the op.amp. to charge it within 40 to 60 ms. The two 100 KΩ trimmers will vary the positions of the leading and trailing edges of the maternal blanking window.

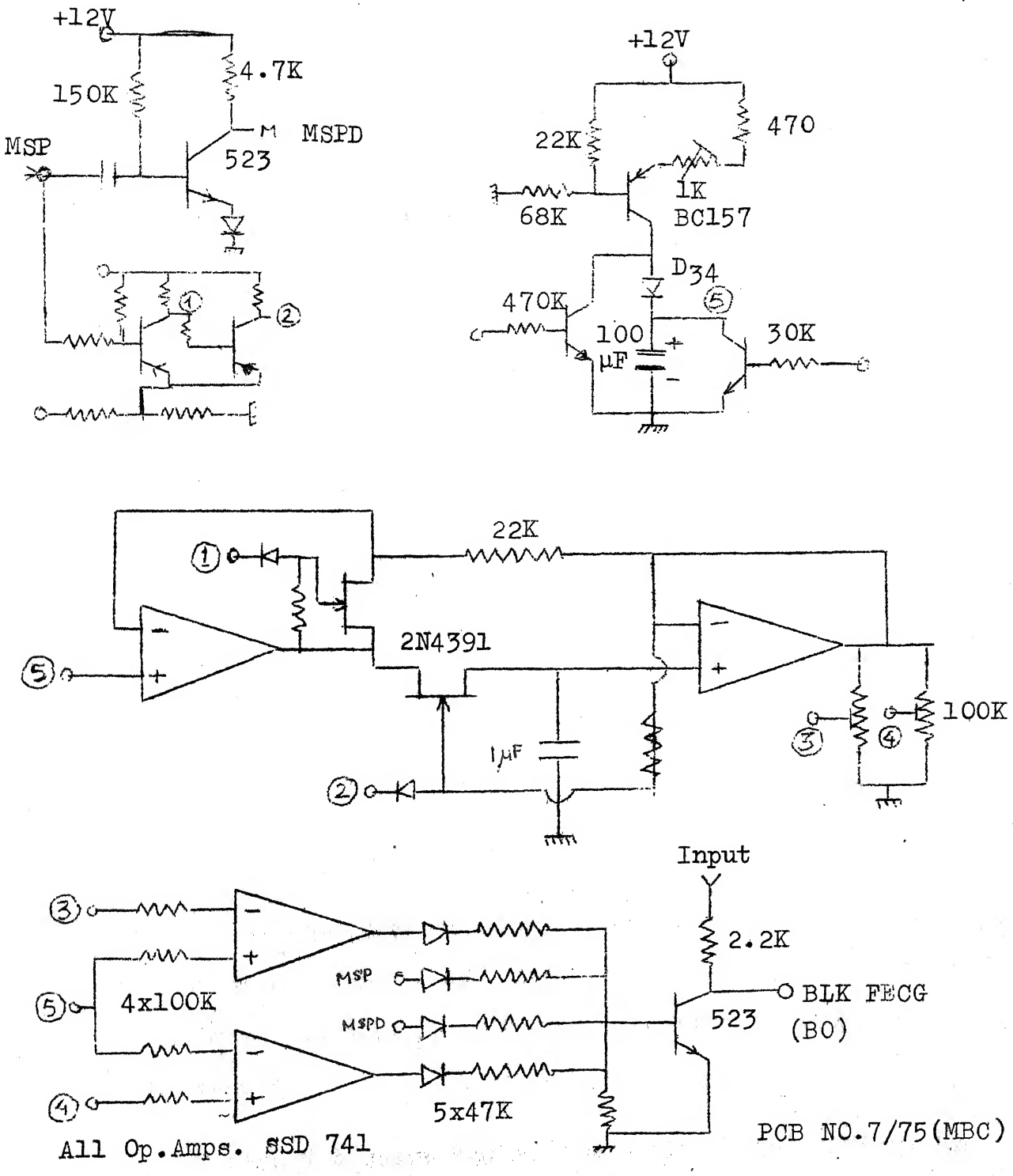


Figure 5.3: MATERNAL BLANKING CIRCUIT.

The MBW is set to the required width when the maternal period is at its minimum (0.5 sec.). The width increases by 20 to 25% when the maternal period reaches its maximum value (1 sec.).

5.4 THE MATCHED FILTER

We need two second order low pass filters with Q's of 0.6 and 1.25. We use the VCVS configuration which is generally used for low Q filters.

For a VCVS low pass filter with identical resistors and capacitors

$$Q = 1/(3-K) \quad \text{or} \quad K = 3 - 1/Q$$

Hence $Q_1 = 0.6$, $K_1 = 1.25$

$Q_2 = 1.25$, $K_2 = 2.2$,

$\omega_o = 162$ rps as calculated in Chapter 3.

$\omega_o = 1/RC = 162$ rps.

Let $C = 0.1\ \mu F$

then $R = 62\ K\Omega$

We use 709 op.amp. for the VCVS as it has a better step response (when properly compensated) than 741. The compensation used is for gain = 1, i.e., 1.5 KΩ and 5 nF at the input and 200 pF at the output.

Figure 5.4 shows the matched filter realisation. We got an output almost similar to the expected impulse response

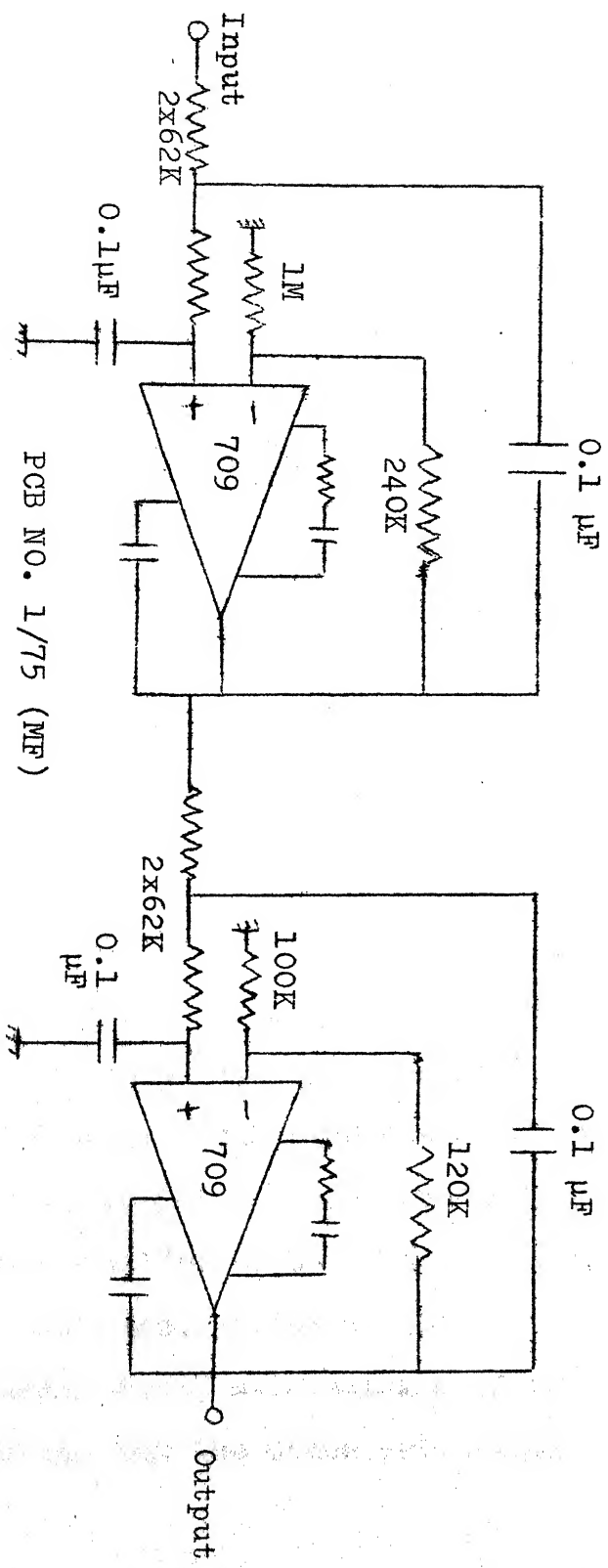


Figure 5.4: THE MATCHED FILTER.

with a 12 volt pulse of 3.5 ms duration. The filter when tested with a simulated foetal signal gave detection delay of 19.6 ms and a signal to noise ratio improvement of more than 10.

5.5 CLIPPER AND PEAK DETECTOR

After the matched filter an op.amp. inverter with a bypass switch is provided, the necessity of which is explained in the last chapter (S is open for positive foetal R peaks). The gain element can give a gain from 1 to 11 so that the peak detector can be provided with peaks of amplitudes much greater than the diode forward voltage. The op.amp. clipper permits only the negative peaks to pass through with an inversion. Thus the base line noise tis not allowed to interfere with the peak detection.

The function of the peak detector is to give the exact instant at which a positive peak occurs. In the circuit shown in Figure 5.5 the op.amp. comparator detects the instant at which the diode D_1 stops conducting and D_2 starts conducting. The comparator output is then inverted and differentiated to give a sharp positive pulse. This output is further gated through a NAND gate having as its control input the output of the clipper shaped by a cascade of two transistor inverters, in order to cut out the diode switchings at the other instants.

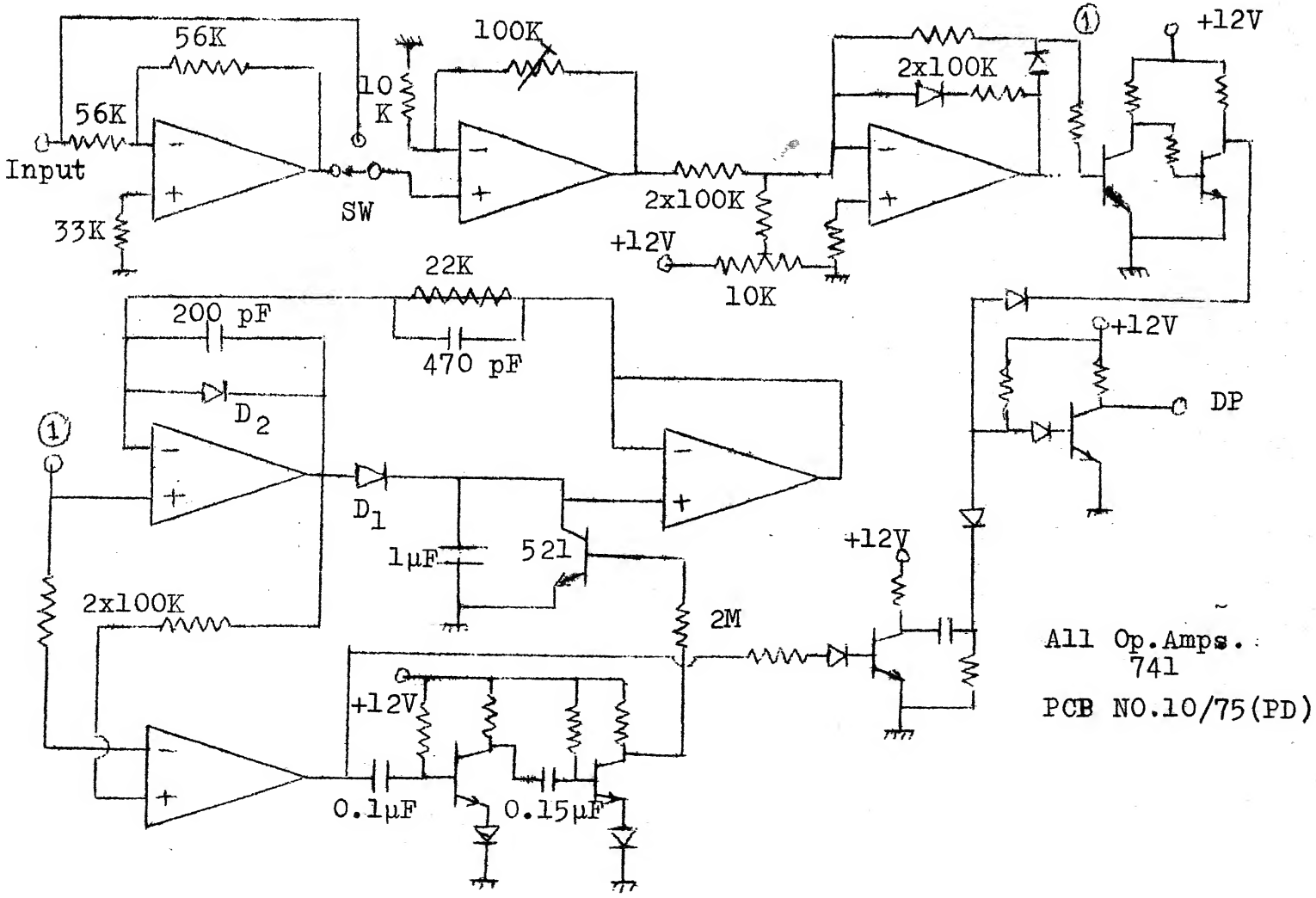


Figure 3.5.5: CLIPPER AND PEAK DETECTOR.

The 200 pF and 470 pF capacitors supress the oscillations and hence the generation of multiple detect pulses, when D_1 and D_2 are both out of conduction. The holding capacitor is discharged after a 50 ms delay which is much greater than the maximum possible width of the input peak (20 ms) and much smaller than the minimum foetal period of 250 ms (240 bpm).

5.6 AUDIO-VISUAL INDICATORS

The detect pulses (DP) thus generated are used to drive a LED and a speaker. Figure 5.6 depicts the driver circuit. A pulsed current of 15 mA and 100 mA is provided to the LED and the speaker, respectively.

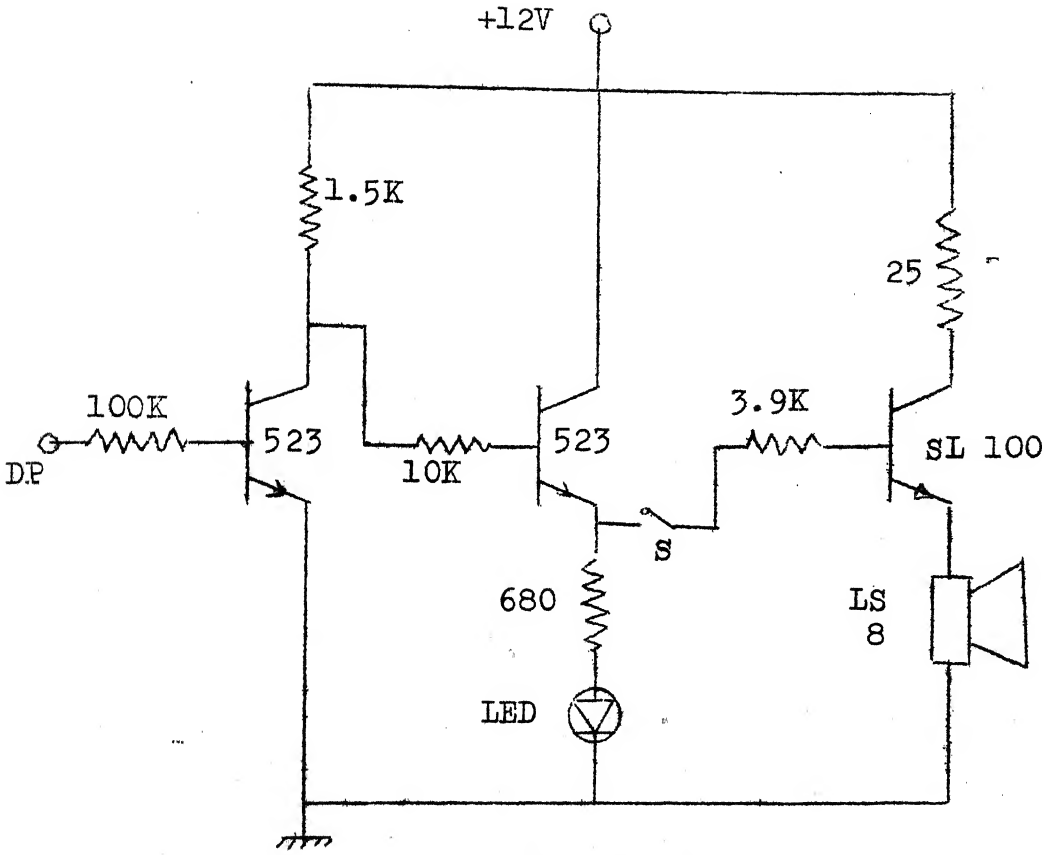


Figure 5.6: LED/LS DRIVER.

Chapter - 6

DIGITAL UNIT - HARDWARE DETAILS

This chapter will deal with the detailed design of the digital unit. The entire circuit is split into six parts. We will consider them one by one along with the logic maps.

6.1 THE A-D CONVERTER AND THE INPUT CIRCUITS

As shown in Figure 6.1, the FECG input (with maternal blanking) from the analog unit is sampled and held for digitization at every sample pulse. The sample pulse is stretched for more than two clock periods (>80 μs). This stretched pulse is given to the synchronized single pulse generator (SSPG), which is needed to correlate the clock pulse generator and the sample pulse generator. The output (T_A) of the SSPG, is used as the A to D conversion delay (minimum). The whole system is reset (excluding the Asynchronous logic generator) with a sharp reset pulse R_1 generated by a monostable which senses the negative edge of T_A. The pulse T_A is then delayed by one clock period with the help of a D flip-flop to get the pulse T_B which is used to shift the A to D output (8 bits including sign bit in 2's complement form) into the Register A (parallel shifting). The time relations of these pulses are shown in Figure 6.3. $\overline{CP.T_B}$ is the parallel shift clock for Register A. For register A we use the parallel in - serial out

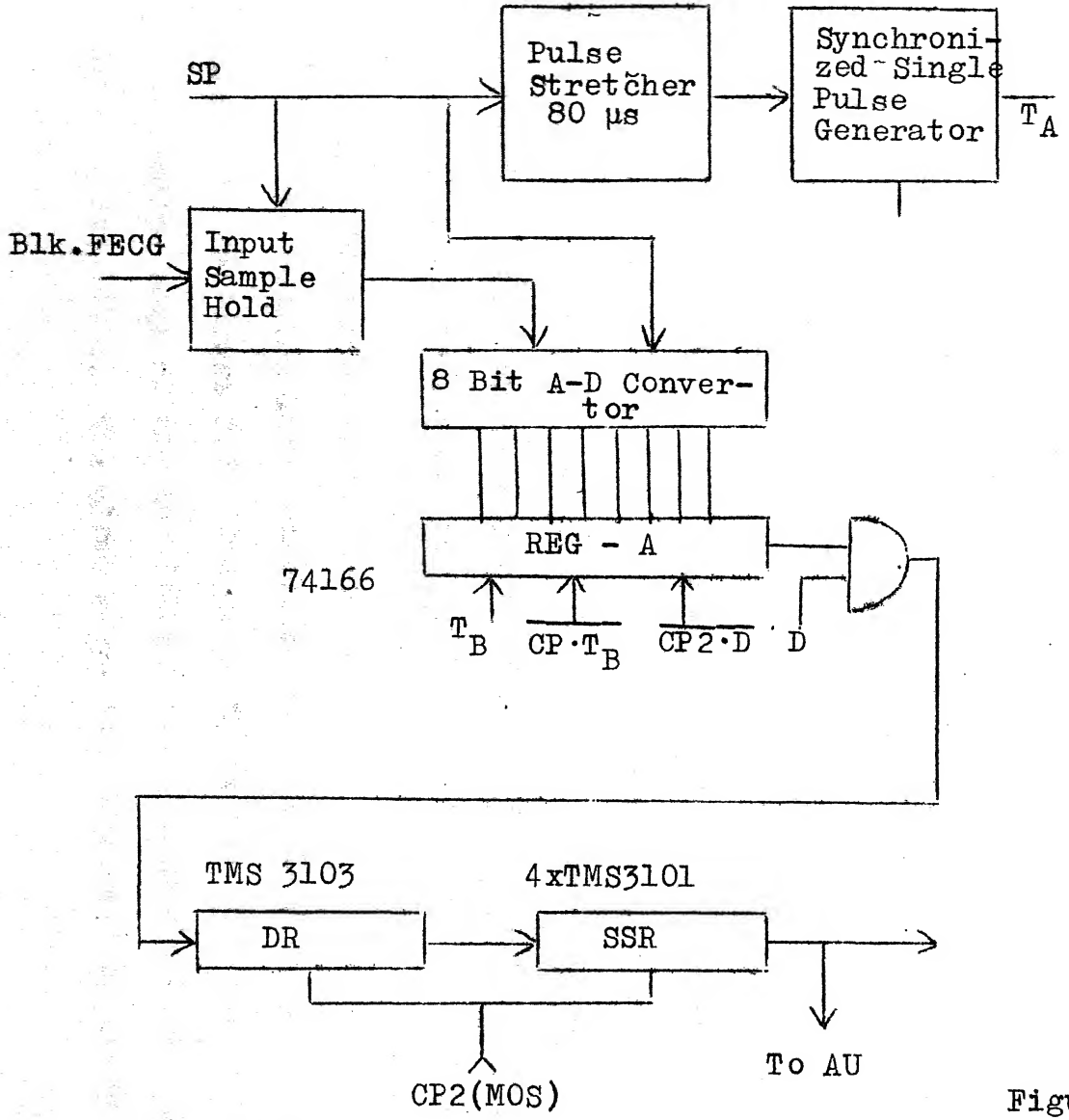


Figure 6.1: A-D CONVERTER AND INPUT CIRCUITS

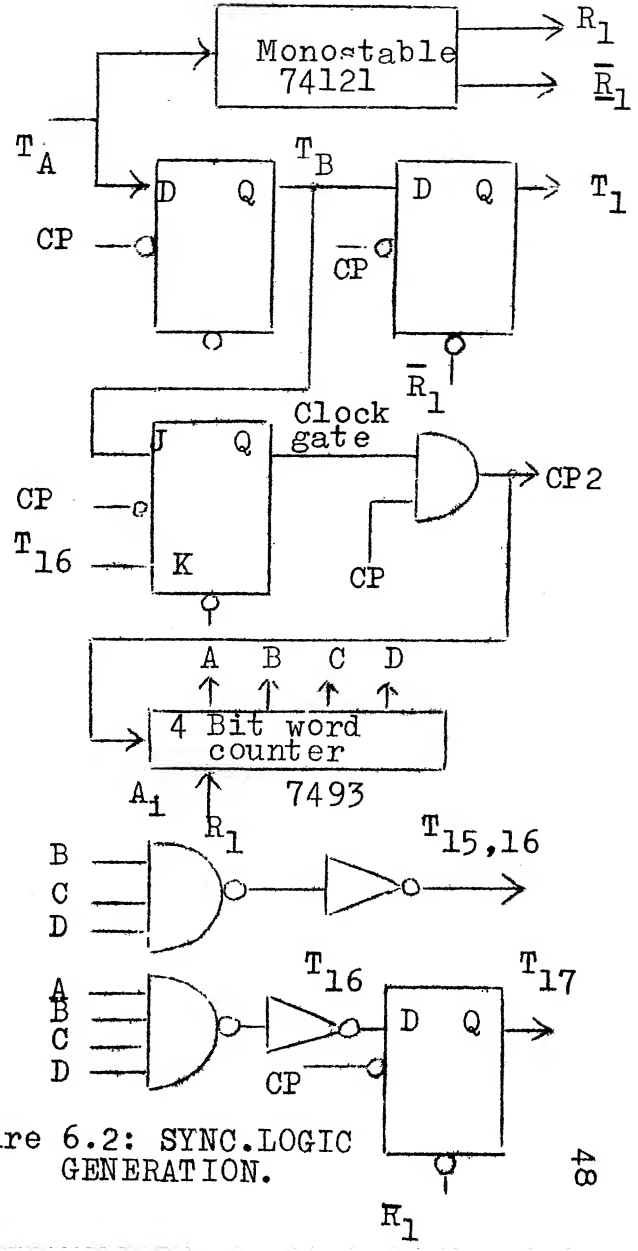


Figure 6.2: SYNC.LOGIC GENERATION.

8 bit shift register SN74166. Eight low-order zeros are to be added to the word now in register A before starting serial shift of the data from register A into DR. This is accomplished as follows. The D output of the 4 bit word counter (shown in Figure 6.2) remains zero for the first half of the 16-pulse clock burst (CP_2) and hence the simple AND gating shown in Figure 6.1 enters 8 zeros into DR during this interval. The serial shift is inhibited for register A during this interval by giving it $\overline{CP_2}.D$ as the serial clock. The register DR is 16 x 8 = 128 bits long so we use the TMS3103, dual 64 bit MOS static shift register., for DR. For register SSR, which is connected in tandem with DR, we need 50 x 16 = 800 bits, so we use 4 chips of TMS3101, the dual 100 bit MOS static shift register. If available, it would be better to use National Semiconductor's MM5058, MOS LSI chip, a 1024 bit static shift register requiring the same power supplies (+5V and -12V), a built-in 3 phase clock generator and clock drivers. A little decoder changes will then be needed in the asynchronous logic generator. The serial output of the SSR either spills out or goes to AU whenever a new complex is detected.

6.2 THE SYNCHRONOUS LOGIC GENERATION

The related logic circuits are given in Figure 6.2 and the plots in Figure 6.3. The pulse T_B is used to generate the leading edge of the 16-bit-long clock gate with the help of a JK flip-flop. The clock burst CP_2 generated by using

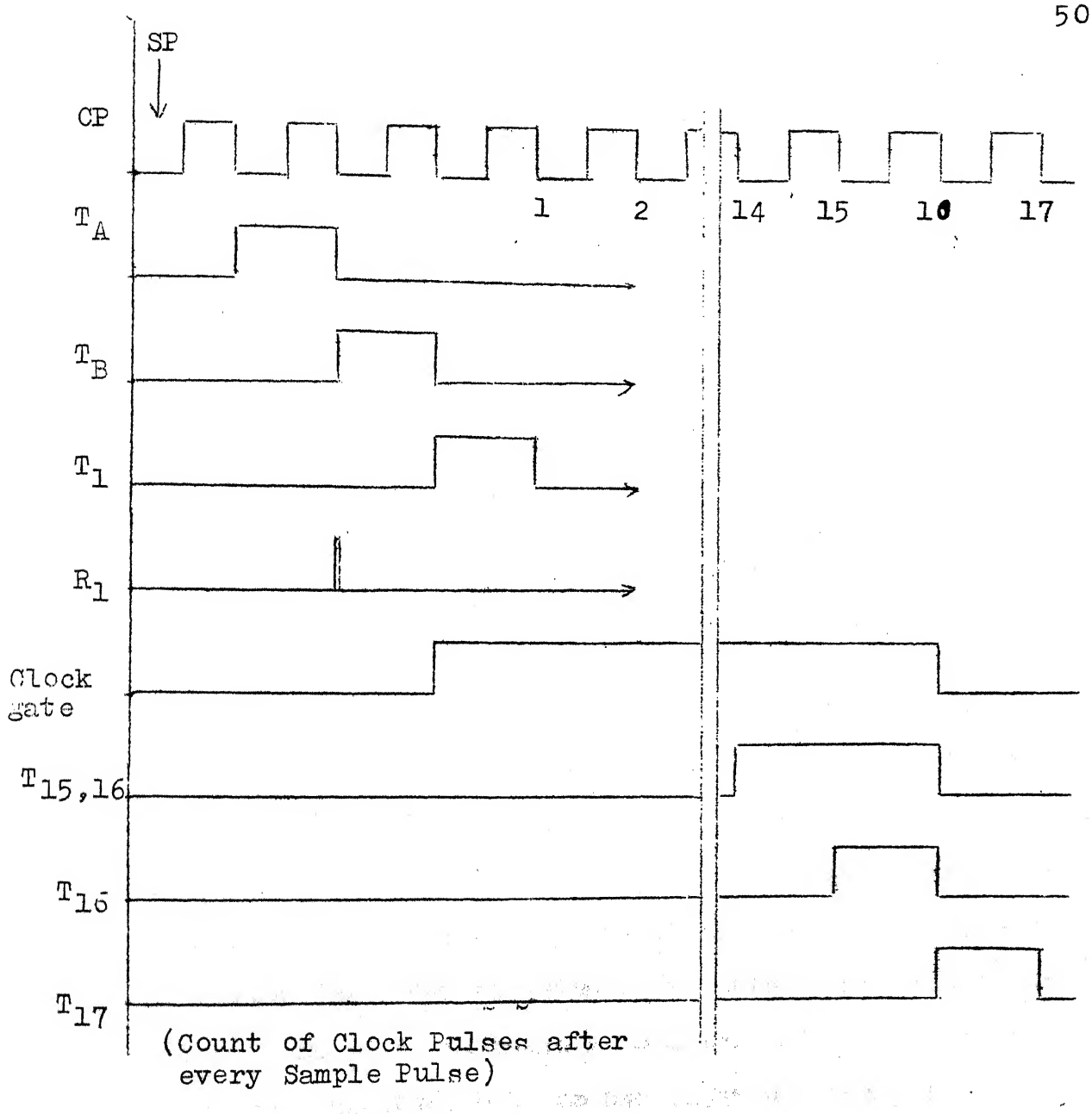
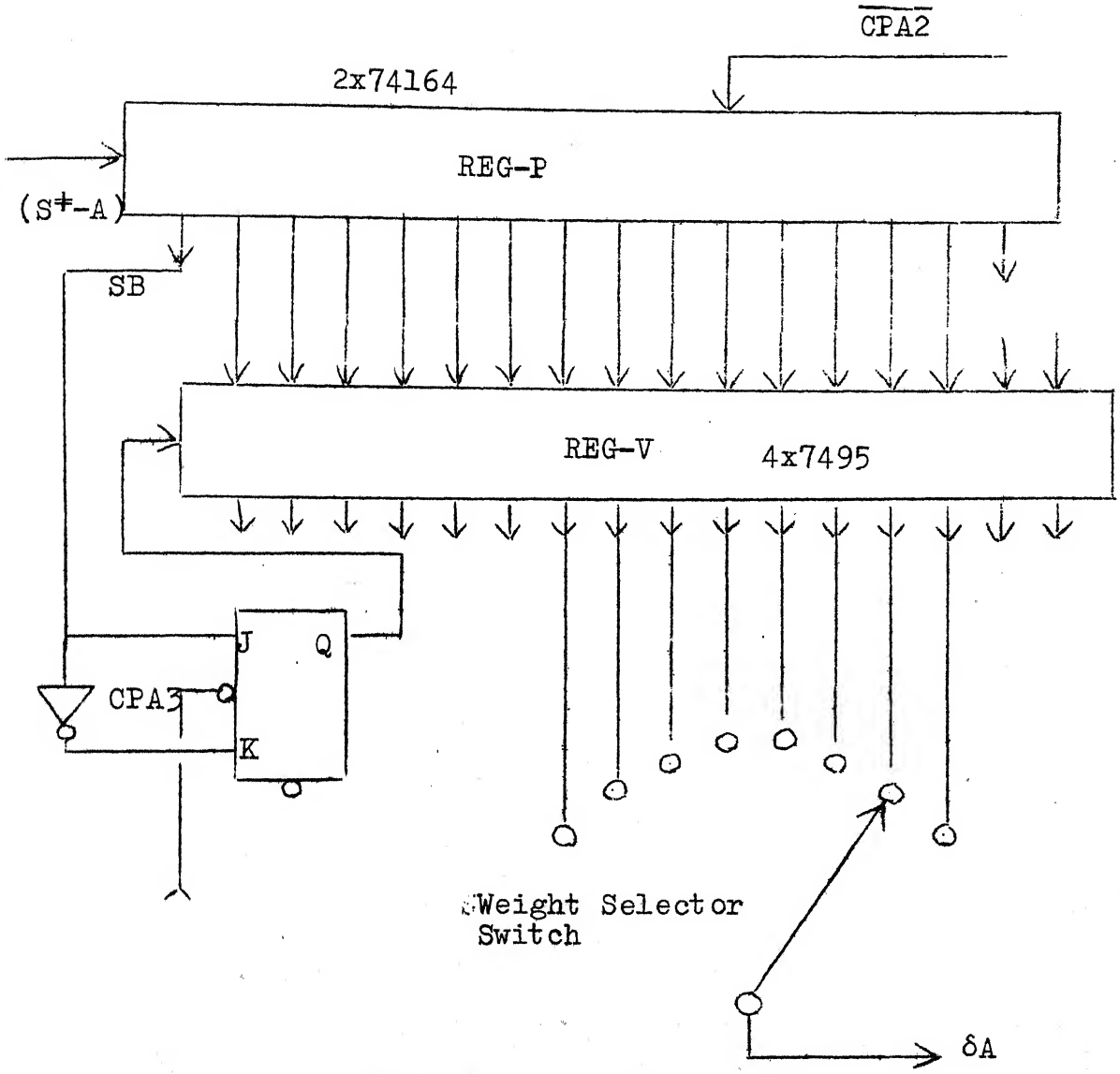


Figure 6.3: SYNCHRONOUS LOGIC MAP.

this clock gate is then fed to the count input of the 4 bit binary counter (word counter) in a single chip (SN7493). The last state of this counter (T_{16}) is decoded by appropriate gates which is then used to reset the clock gate. T_1 is the delayed version of T_B, needed for recomplementing in AU and T_{17} is the delayed version of T_{16}, needed for the output sample and hold. $T_{15,16}$ is also needed for recomplementing in AU.

6.3 THE ARITHMETIC UNIT

This unit has to perform the operation given by eqn.(4.2). For the subtraction (S^*-A), the MSR output (A) is complemented by a flip-flop-Ex-OR circuit and then added to the SSR output (S^*) by a gated full adder chip SN7480 in conjunction with a JK flip-flop and a NOT gate. The register MSR has the same structure as SSR, described in Sec. 6.1. The circuit for the AU is spread on to three figures: 6.4, 6.5 and 6.6. The quantity (S^*-A) is then shifted serially into register P for division by M. Since $M = 2^n$ (n=1 to 8) all we need to do is to hold back the sign bit (the last bit), shift the magnitude bits to the right n times, then shift n bits identical to the sign bit and finally shift the sign bit too. This will require one word of time. Hence the word that has been shifted into register P will be parallelly shifted into register V during T_{17}. The division operation



For REG-V:

Serial Shift: CPA2 = CP2.ARTH

Parallel Shift: CPA3 = $CP \cdot T_{17} \cdot ARTH$

Mode Control: T_{17}

PCB NO. 41/75

Figure 6.4 THE DIVIDER CIRCUIT.

will be performed on this word during the next burst of clock pulses. The sign bit of course, is shifted into separate flip-flop so that we can hold it back. The value of M will depend upon which of the parallel outputs of register V is used to tap off the word serially. A one-pole eight-throw weight selector switch can perform this function. Thus we get δA at the pole point of this switch. We use two chips of SN74164, the 8 bit serial in-parallel out shift register for register P and four chips of SN7495, the 4 bit parallel parallel out shift register for register V.

Mean while, the output of MSR, A, is delayed by one word through register B to compensate for the division delay. The serial output of register B is then added to the output of the divider by another full adder. This full adder gives in 2's complement form at its output. Since the D to A needs sign-magnitude form we need to complement A' before display. This requires the sensing of the sign bit which thus forces us to put another one word register F before we close the memory loop, i.e. return A' to the input of MSR. The pulse T_1 is to sense the sign bit which is then used to set a latch. If the sign bit is '0' the latch clears the flip-flop for a durat of one word so that the particular word passes through the complementor to register D as it is. While a '1' sign bit prevents the latch from clearing the flip-flop and the word is complemented as usual. The pulse $T_{15,16}$ prevents the

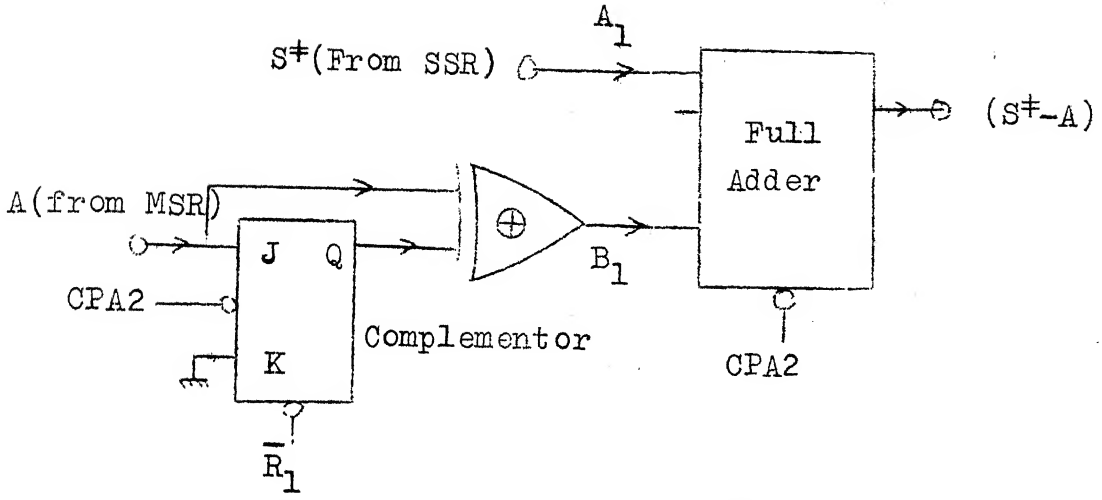


Figure 6.5(a): THE ADDER AND COMPLEMENTOR.

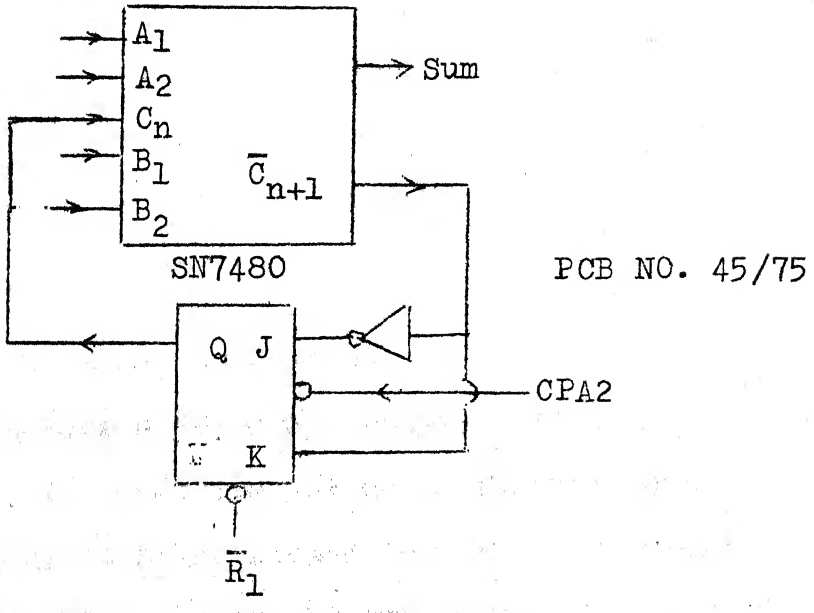


Figure 6.5(b): FULL ADDER DETAILS.

complementing of the sign bit itself, irrespective of whether the sign bit is '1' or '0'. The output of the recomplementor shifts serially into register D whose parallel outputs are connected to the D to A converter. The output of the D to A converter is sampled only during T_{17} to drive the display device, e.g. a strip chart recorder. Since the output of the sample and hold is required only during the display interval we use a transistor switch in shunt to gate the same.

The whole arithmetic unit gets the serial shift clock CPA_2 only during the arithmetic interval. CPA_3 is a clock pulse used for parallel shifting of the word from register P to sign bit flip-flop and register V. CPA_2 has to be passed through a clockdriver to generate a two phase clock for MSR. We use 2 chips of SN7491, the serial in-serial out shift register for register B and one chip each of SN74164 and SN7491 for register F. For register D we again use SN74164.

6.4 ASYNCHRONOUS LOGIC GENERATION

Here we have a 50-word complex. The Detect Pulse (DP) indicates that 25 words are yet to be shifted into SSR, so that a foetal complex is fully loaded into it. A DP starts the sample counter which counts the sample pulses. The 26th sample pulse opens the Arithmetic (ARTH) gate (Figure 6.8). Now, our memory loop consists of 52 words, 50 words in MSR and one word each in the divider and the recomplementor. Hence, display

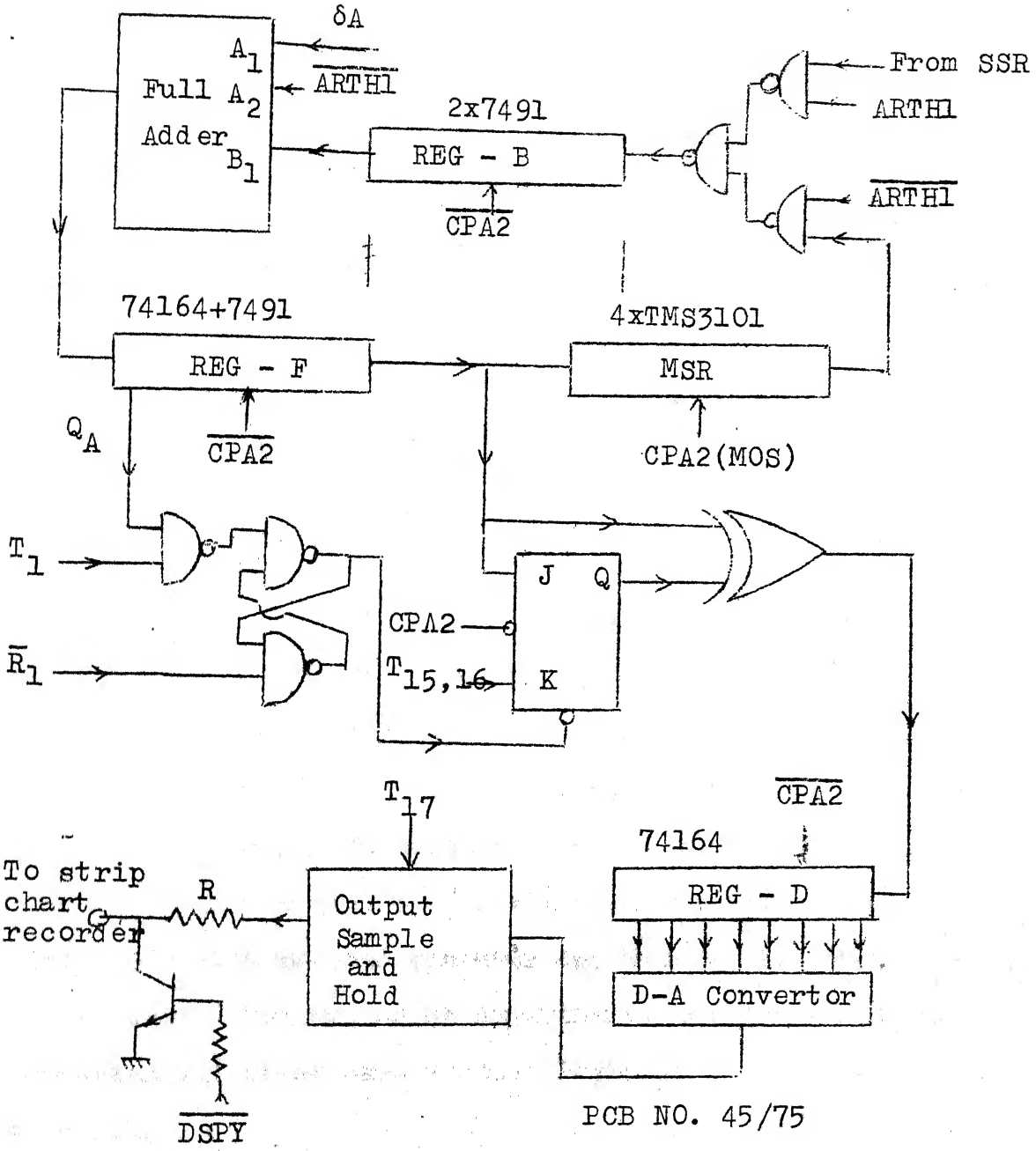


Figure 6.6: THE RECOMPLEMENTOR, MEMORY LOOP AND OUTPUT CIRCUITS.

starts two words later than the start of ARTH. The display gate (DSPY) is thus opened after the 28th pulse arrives. Since all the 50 words in SSR have to get into computation and display, these gate pulses will end only after 77 sample counts. The 78th state has therefore to be detected and used to reset all the asynchronous logic including the sample counter. The pulses CT1, CT2 and CT3 are the decoder outputs which go high during 26th, 28th and 78th sample count respectively.

The manual reset triggers a monostable (SN74121) which generates a pulse and is used to reset all the asynchronous logic whenever desired. The PR1 is the combined reset pulse for the system. The manual reset is also used to open a gate ARTH1 (usually it is the first ARTH pulse). Referring to Figure 6.6, it is clear that ARTH1 stops all the arithmetic and fills the MSR directly by the contents of SSR. Thus the first complex that is detected can be put directly into MSR, in readiness for averaging with the next complex. This facility can also be used whenever one desires to remove the old contents of MSR during an experiment. We use NOR latches to generate all these asynchronous logic as shown in Figure 6.7.

The sample pulses are generated by a negative resistance oscillator which is quite capable of giving sharp pulses of low duty cycle. The sample rate is kept variable from 2 to 3 ms and the pulse width is less than 10 μs.

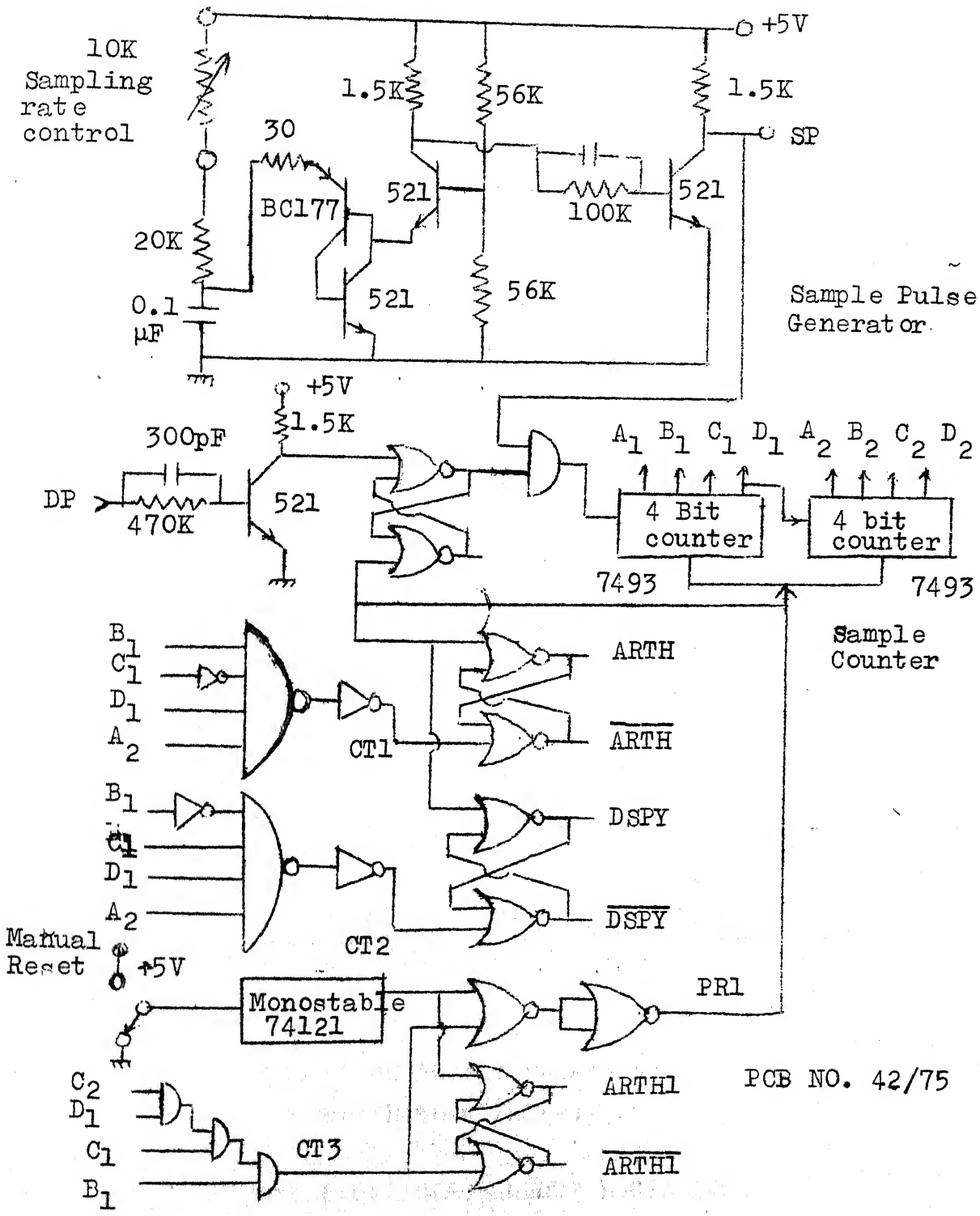


Figure 6.7: ASYNCHRONOUS LOGIC GENERATOR.